HITACHI Analog·Hybrid Computer

Technical Information Series No.5

PROGRAM MANUAL FOR HITACHI ANALOGUE COMPUTER

—AUTOMATIC PROGRAMING—

1968

Hitachi, Ltd.

printed in Japan

CONTENTS

1. Description

An automatic system is defined as a system which automatically analyzes problems pertaining to so-called parameter optimization such as problems of boundary value, extreme value, etc. which in the past usually had to be solved by a trial method when using conventional analogue computers. In this system, a digital logic element is added to the analogue computer. With this arrangement, it is possible to analyze those complicated problems, and the various settings and controls which have been conventionally performed under manual operations can now be performed automatically, thereby increasing the functional capability of computation. The method of programing to which this system is applied is called Automatic Programing. It has been said that obtaining an initial value or unknown coefficient to have a given equation satisfy the rated boundary conditions is somehow troublesome and even time waisting. Under an automatic system, however, the entirely mechanical operation (called Trial Method) which was conventionally performed by human beings is now entirely performable by an automatic system. For example, when deciding a unknown parameter included in an equation by boundary conditions, the parameter is properly and temporarily decided, computation is performed based on the temporary parameter, the difference between the results of the computation and the boundary value is detected, the parameter is automatically corrected by the computer itself with a proper evaluating function, and the computation is reperformed. The value of the parameter is gradually converged to the true value by repeating such operations as described above. However, when performing programing to which this automatic system is applied, some basic knowledge pertaining to the logic operation circuit on an analogue computer is required. At the same time, it must be so remembered that a considerably high programing technique is required when numbers of unknown parameters are involved. The following are analysis examples achieved by various solution method. In the following examples, an equation of a boundary value having only one variation is used.

(Example)

$y'' + ay' + 4y = 0$

Obtaining value of "a" with which the following conditions are satisfied:

$y = 0.5, \quad y' = 0 \quad$ when $t = 0$

$y = 0.1, \quad y' = 0 \quad$ when $t = t_1$

(Solution)

(1) Manually correcting operation

(Trial method)

In Fig. 1.1, block diagram, the value of "a" is sought by a trial and error method through computations one by one.

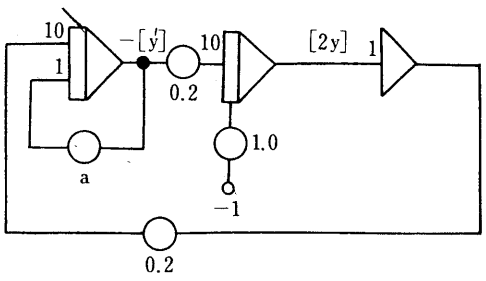


Fig. 1.1 Block Diagram by Trial Method

When an analogue computer which has high speed repetitive operation capability is used, solving a problem is possible even for 2 to 3 parameters. However, when employing a low-speed type analogue computer, solution of multiple variations is practically impossible.

(2) Method in which an automatic system is used.

In this method, a computing group to correct parameter is required in addition to the main computing group.

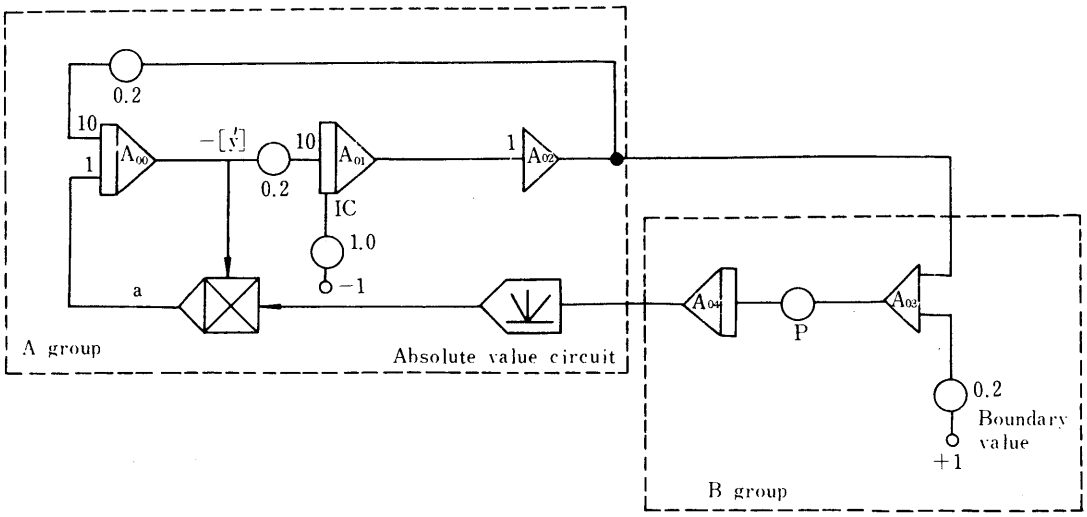


Fig. 1.2 Block Diagram in which Automatic System is Applied

In Fig. 1.2 above, the computing modules which belong to the A group compose the main computing circuit which resolves the given equation, and the B group is an auxiliary computing circuit which performs correcting of parameter "a".

Mode controls of the A and B groups can be made independently, and mode controls of the these two groups pertaining to this equation are decided as shown in the table in Fig. 1.2. More specifically, when starting computation, the value of the parameter "a" is held to any desired value (zero-volt in this case), and the A group is computed. Next, the A group is temporarily held, the difference between the value of the held "-2y" and "+0.2 (+20V) -- the boundary value -- is detected by summer "A03", and this value is corrected and integrated by the integrator unit "A04".

After integrating for a certain time, "a" is held again, and the A group performs computation for a "t_1" second again based on the newly corrected value of "a". As described above, low-speed computations are repeated, and the final value of "a" will be obtained.

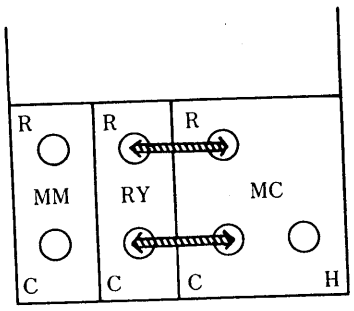
R: Reset

C: Compute

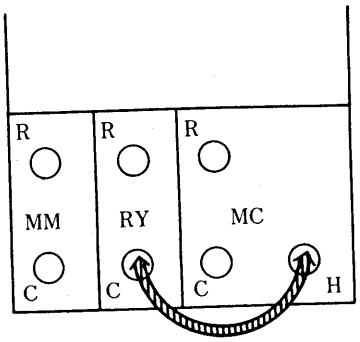
H: Hold

Now, referring to the terminations on the patch board, how to prepare a logic control mode is explained below.

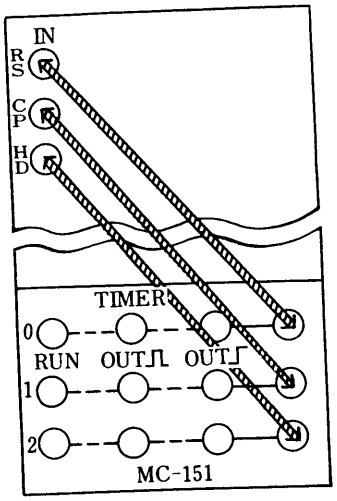
For A group integrator unit control



For B group integrator unit control



When Mode Control (MC) is controlled by timer TM-251:



(3) Sample hold system

Sample Hold Device (it is possible to assemble this device on a patch board by using general purpose amplifiers) is employed in this system, combined with a repetitive operation for having a correcting operation.

The flow chart is a shown below.

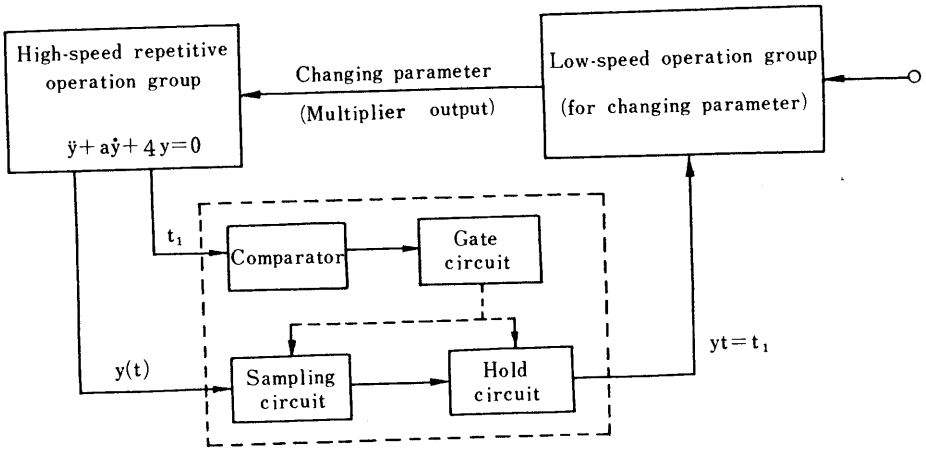


Fig. 1.4 Automatic Operation by Sample Hold System

The features of this system are that speed available to approach an unknown parameter is extremely high (since the main operational group is operated under high speed), and that a logic circuit can be established comparatively rather simply by using a special unit in the portion encircled by a dotted line. It may be slightly complicated; however, a circuit diagram when a sampling hold unit is assembled on a patch board is shown in Fig. 1.5.

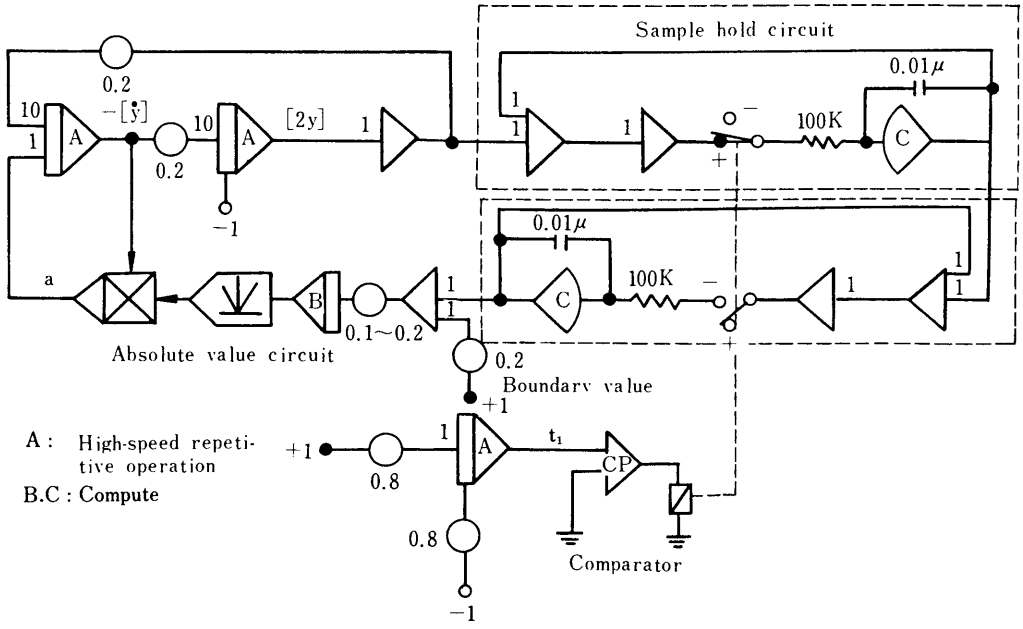


Fig. 1.5 Program Utilizing Sample Hold Circuit

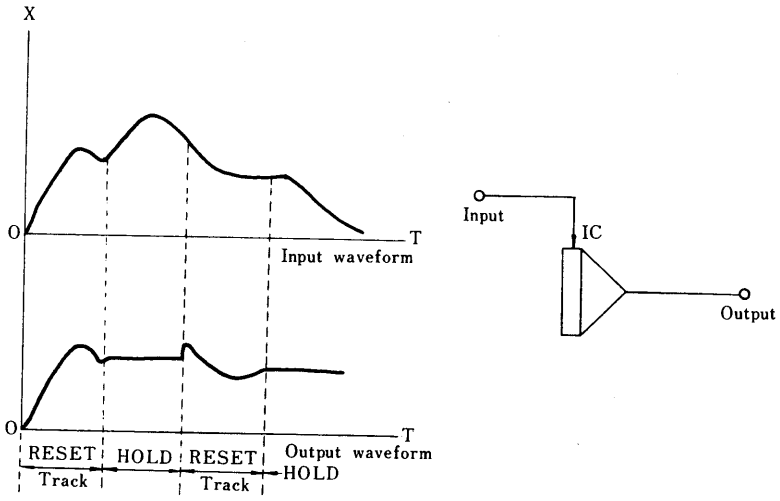
2. Logic Operation Circuit

Both description and types of basic logic circuits used in automatic programing are limited in some ranges, and they consist of several kinds of memory elements (mainly integrators), a operation control circuit, a relay circuit, and so on.

2.1 Memory element

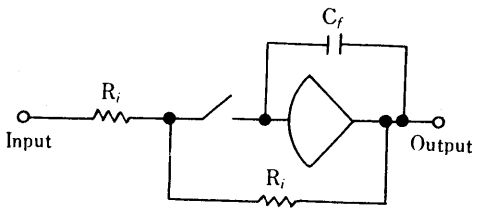
(1) Trank hold

In this hold system, the IC input terminal of the integrator is utilized as a primary delay circuit, and this system has the functions shown in the following diagram.



(2) Sample hold

In this system, there are two different ways to compose the circuit. One is exactly the same as the track hold as far as the circuit is concerned. However, setting can be made freely by combining an integrator and operational impedance. Moreover, a similar circuit can be composed by combining an inverter with a relay. The relations between operation mode and the sample/hold are shown below.



	Follw-up	Memorize
Integrator	COMPUTE	HOLD
Inveter	Relay ON	Relay OFF

Fig. 2.2 Sample Hold Circuit

The other sample hold circuit is shown in Fig. 2.3, in which one integrator unit and two summers are used. However, operations (COMP - FOLLOW-UP and HOLD-MEMORY) are the same.

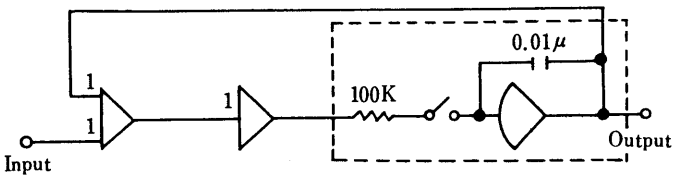


Fig. 2.3 Sample Hold Circuit

In this diagram, the follow-up time constant is 0.001S; thus, it should be noted that the hold characteristics become unsatisfactory when this time constant is excessively reduced. In addition to the above, a sample hold can be performed simply by using an electronic switch, Type CP-153, High-Speed Comparator.

(3) Maximum value holder

In this circuit, maximum value of the input signal can always be obtained on the output by applying a signal to the input. For example, when a signal as shown in Fig. 2.4(a) is applied to the input, the output waveform appears as shown in (b). Also, there are three different ways in which the method can compose this circuit, as illustrated in Fig. 2.5(a), (b), and (c).

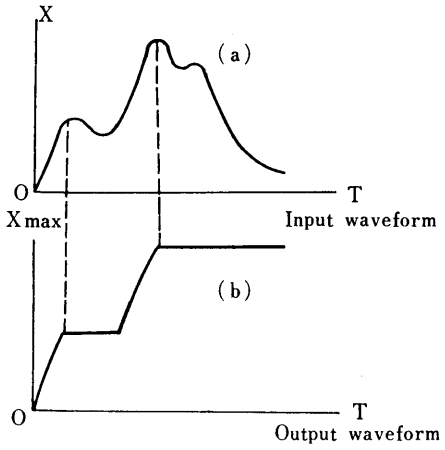


Fig. 2.4 Input and Output of Maximum Value Holder

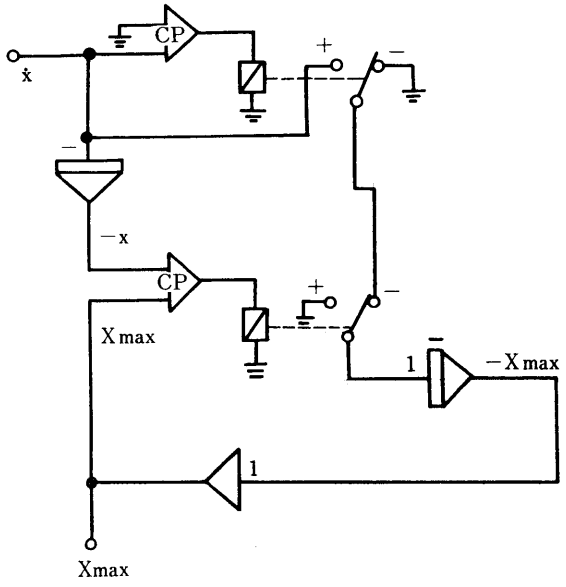


Fig. 2.5(a) Maximum Value Holder Circuit

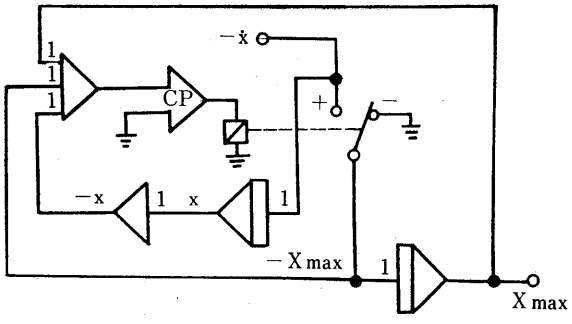


Fig. 2.5(b) Maximum Value Holder Circuit

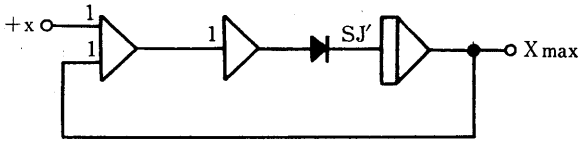


Fig. 2.5(c) Maximum Value Holder Circuit

2.2 Logic circuit for operation control

The methods of controlling repetitive operation can be classified into the following three types:

Method using a timer
Method using a digital logic panel
Method combining a DC amplifier and a comparator

The method in which a timer is used is extremely simple; consequently, in this manual, only the remaining two methods will be explained.

(1) Reset-t_1-second and Comp-t_2-second Repetitive Operation

Reset time cannot be freely set on TM-253 timer. However, it is possible when a TM-251 timer is used. When no TM-251 is available, both Reset and Comp times can be made into a freely independent variable by using a potentiometer and employing the circuit illustrated in Fig. 2.7. Repeating calculations are started as soon as the function switch is set from RESET to START.

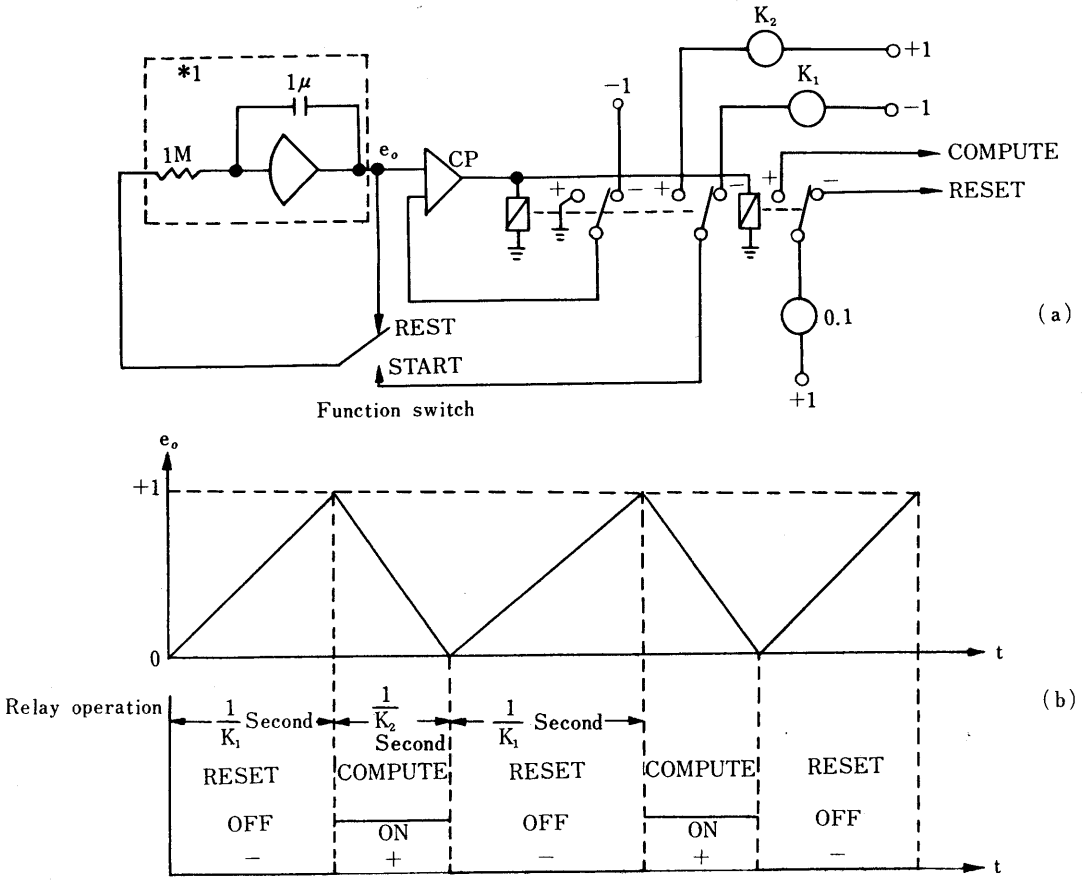
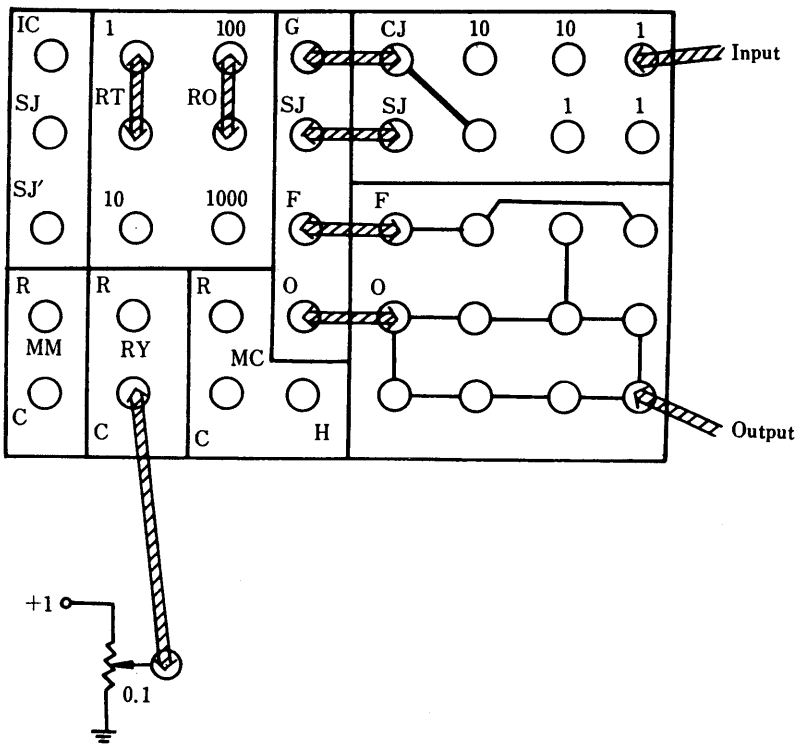


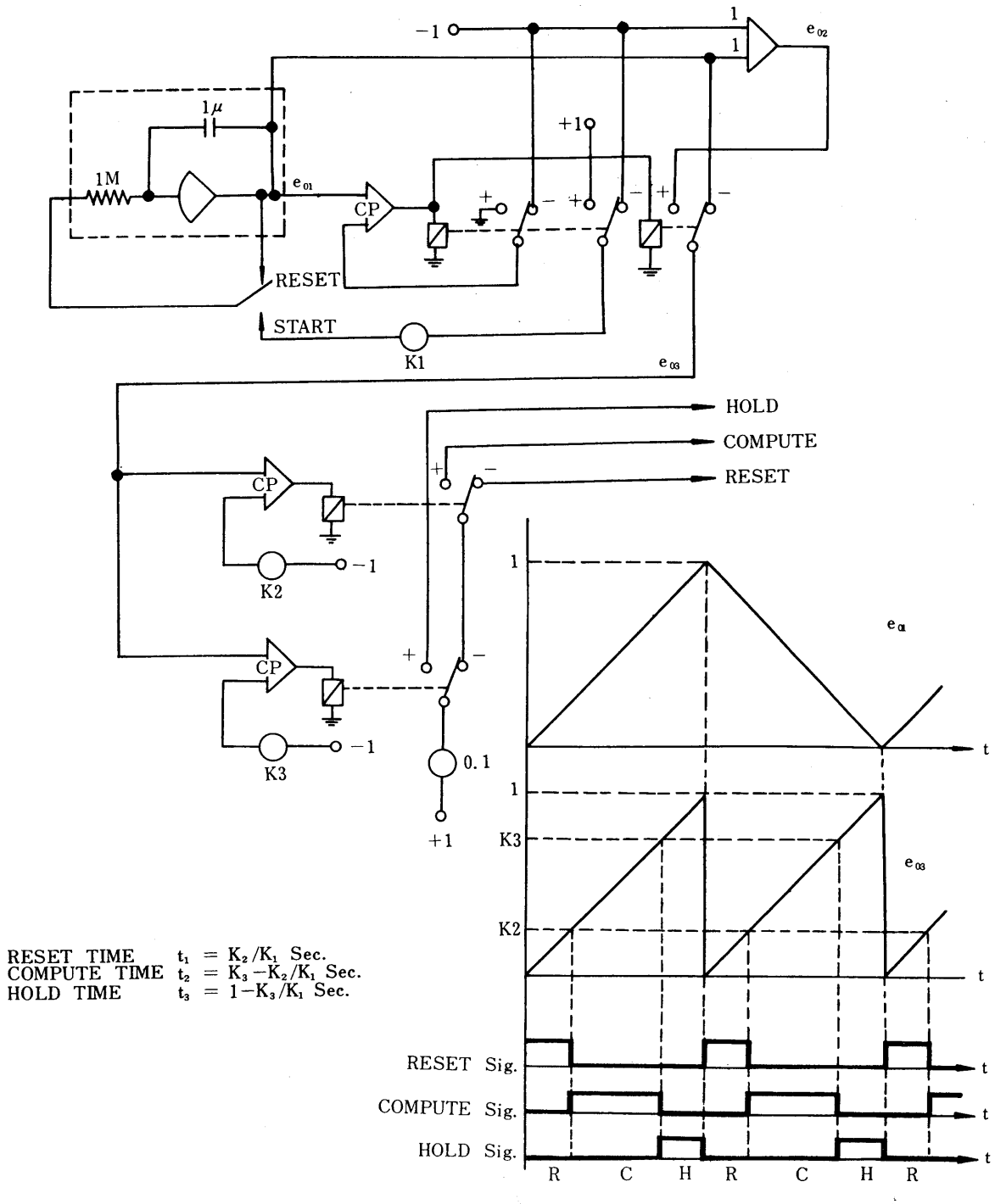
Fig. 2.7 Reset Comp Repetitive Operation Control

(2) Reset-t_1, Comp-t_2, Hold-t_3 Secon Repetive Operation

With this logic circuit, it is possible to perform repetitive operations of Reset-Comp-Hold; also it is feasible to freely set the individual control mode times.

* Wiring of 1 (Refer to Fig. 2.7 and Fig. 2.8)





RESET TIME $t_1 = K_2/K_1$ Sec.
COMPUTE TIME $t_2 = K_3 - K_2/K_1$ Sec.
HOLD TIME $t_3 = 1 - K_3/K_1$ Sec.

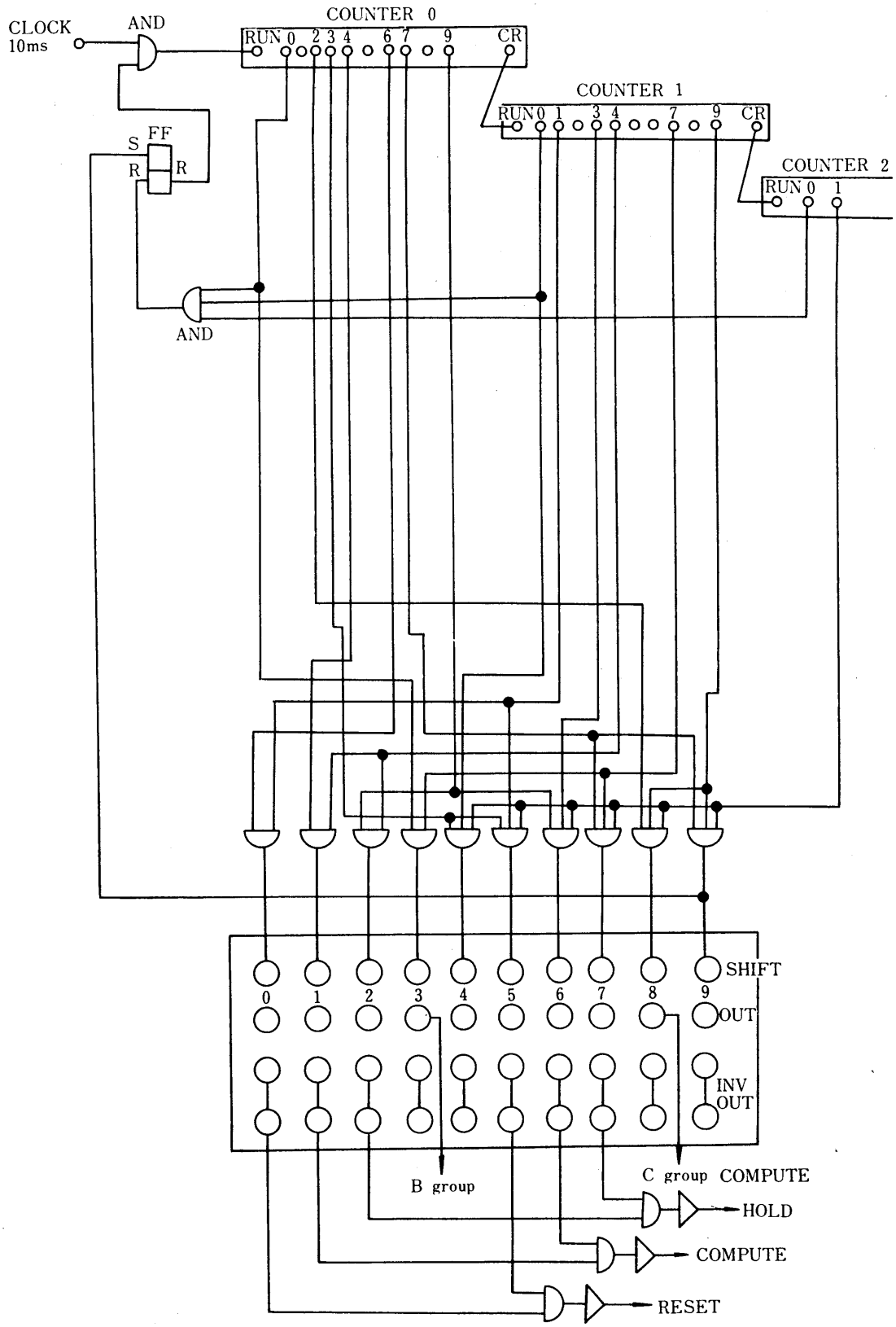
Fig. 2.8 Reset-COMP-Hold Repetitive Operation Logic Circuit and Operating Principle Diagram

The control is started as soon as the function switch is set to START in this theoretical circuit, in a manner identical to (1) above.
The individual mode times are shown above.

(3) Logic Circuit for Repetitive Operation

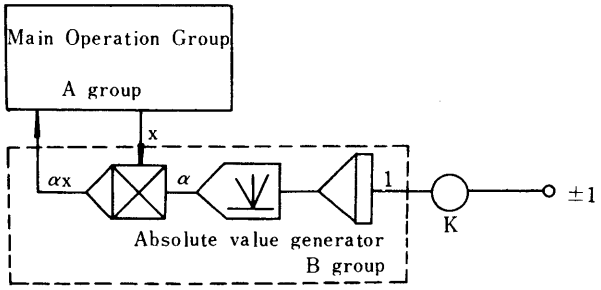
Using time is decided through a combination of counter, logic gate and flip-flop; and by operating the ring counter, different controls having any desired time width within ten types can be produced. Deciding the individual control times:

Time / Product	Setting Time	Total Time	Necessary Operation
0	0.16 Second	0.16 Second	MAIN RESET
1	0.28 Second	0.44 Second	MAIN COMPUTER
2	0.05 Second	0.49 Second	MAIN HOLD
3	0.21 Second	0.70 Second	B GROUP COMPUTE
4	0.33 Second	1.03 Second	B GROUP HOLD
5	0.10 Second	1.13 Second	MAIN RESET
6	0.26 Second	1.39 Second	MAIN COMPUTE
7	0.38 Second	1.77 Second	MAIN HOLD
8	0.15 Second	1.92 Second	C GROUP COMPUTE
9	0.05 Second	1.97 Second	C GROUP HOLD


CLOCK
10ms
AND
COUNTER 0
RUN 0 2 3 4 6 7 9 CR
COUNTER 1
RUN 0 1 3 4 7 9 CR
COUNTER 2
RUN 0 1
S FF
R R
AND
SHIFT
0 1 2 3 4 5 6 7 8 9 OUT
INV OUT
B group
C group COMPUTE
HOLD
COMPUTE
RESET

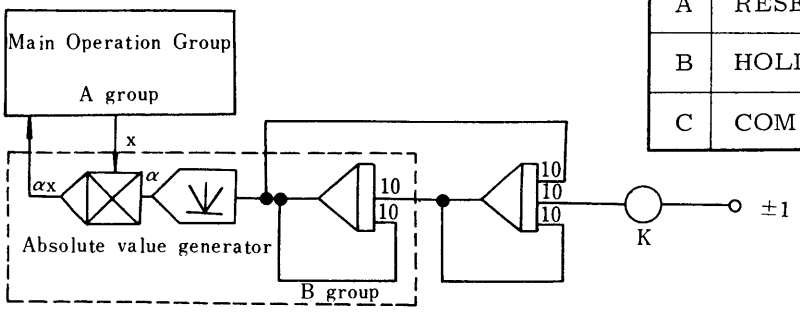
2.3 Other logic circuits for controlling

(1) The logic circuit diagram indicated below is to solve a problem which has one unknown parameter. The parameter on this diagram is continually changed during the logic operation.



	△t	t
A	RESET	COMP
B	COMP	HOLD

Fig. 2.11 Logic Circuit for Parameter Change (1)



	△t	t
A	RESET	COMP
B	HOLD	COMP
C	COMP	HOLD

Fig. 2.12 Logic Circuit for Parameter Change (2)

The difference between the above two logic circuits is that, in Fig. 2.11, the change interval of α is affected by the reset time of the A group; but in Fig. 2.12, the change interval of α is decided only by the value of "k" regardless of the reset time of group A.

2.4 Logic circuit for analysis of boundary value equation

In most cases, a multi-boundary value equation is permited to the extreme value by deciding a proper evaluating function. Thus, in this chapter, the logic circuit is observed by limiting problems to the boundary value with 1 - 2 variables. The logic circuits utilized in this type of equation analysis can be primarily classified into the following three types:

(i) Repetitive operation utilizing track hold
(ii) Repetitive operation
(iii) Repetitive operation utilizing a primary delay network.

These three methods have both individual features and faults; therefore, the appropriate method should be applied after grasping a description of the equation.
The following logic circuits have been devised in order to analyze an unknown parameter automatically in such a manner that the boundary condition "$y = y_t$" is satisfied when $t + t_1$:

	$\triangle t$	t_1
A group	RESET	COMP
B group	HOLD	RESET
C group	COMP	HOLD

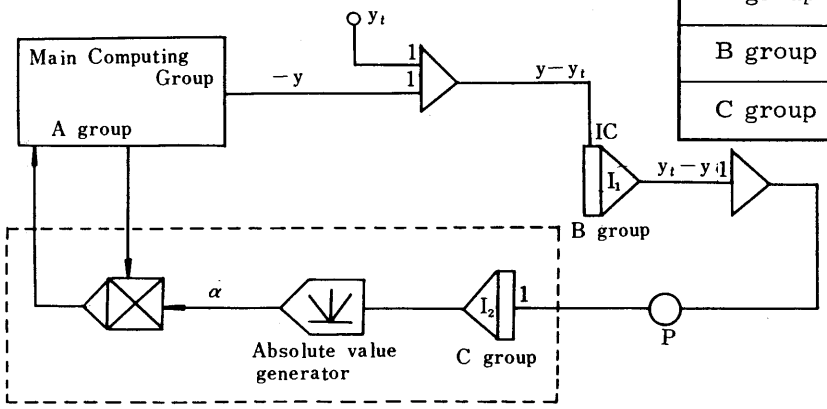


Fig. 2.14 Logic Circuit for Analysis of Boundary Value Equation (1)

In Fig. 2.14, integrator I_1 of the track hold is used for the memory element. Accordingly, the time constant of integrator I_1 must be sufficiently smaller in comparison to that of the main computing group.

	t_1	t_2	t_3
A group	RESET	COMP	HOLD
B group	HOLD	HOLD	COMP

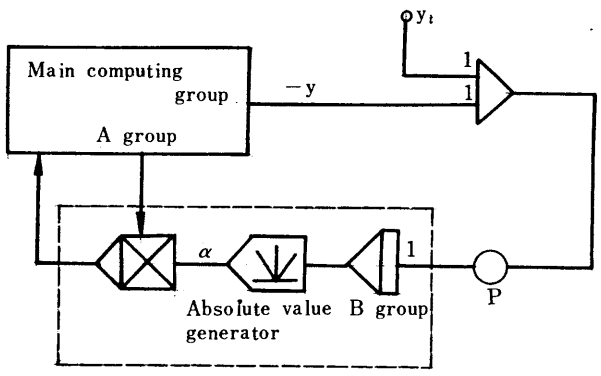
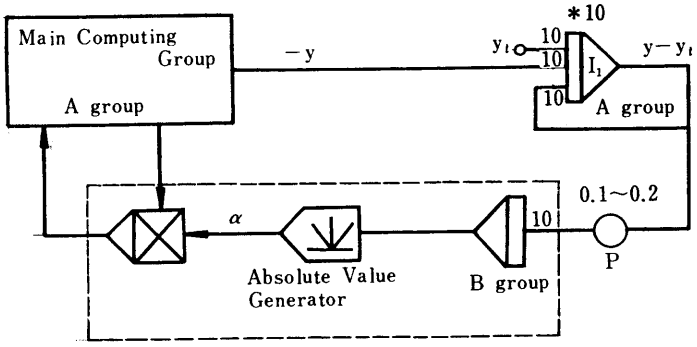


Fig. 2.16 Logic Circuit for Analysis of Boundary Value Equation (2)

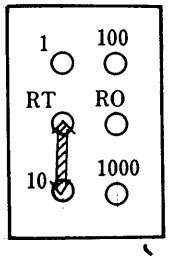
The features of this system are that no errors are made because the time constant of the memory circuit does not affect the system (in Fig. 2.14, the time constant affects operation), and that the number of mode sharing grouo of integrators can be minimized. Among these three types of logic circuits, the third one can obtain the converged value of α with minimum error.



	Δt	t_1
A group	RESET	COMP
B group	COMP	HOLD

Fig. 2.17 Logic Circuit for Analysis of Boundary Value Equation (3)

* 10 indicates that the integrating time constant is 10.



In this system, reset trangent voltage of integrator I_1 is integrated by integrator I_2 in the B group, and the parameter α is corrected. Integrator I_2 corrects and integrates a value in proportional to the tolerance $y-y_t$. Both the COMP and RESET time constants of integrator I_1 are 0.01 second.

In comparison with Fig. 2.14, this circuit can be applied even in the time constant of y is considerably smaller.

The scope of application of those three circuit systems explained above differs individually, depending on the wave forms of the planned "y". Moreover, in Figs. 2.14 and 2.17, because of repetitive operation controlled by the timers, sufficient consideration must also be given to the time-setting error of the timer. Calibration for the setting time of the timer with an oscilloscope or synchroscope is recommended) in the case of a 2-point boundary value question in which two unknown parameters are involved, analysis is still possible by connecting two of the above-described logic circuits in parallel with one main computing circuit group. However, no mutual relation is given to those two parameters, and they are independently controlled. Thus, the tendency is that considerably excessive time is spent in comparison with the steepest descent method described in the following paragraph. In addition, when the number of unknown parameters is three or more, it becomes extremely difficult to approximate. Consequently, in this case, it is better to obtain a proper evaluating function and to permute to an extreme value equation. The method of permutation is described in the next paragraph.

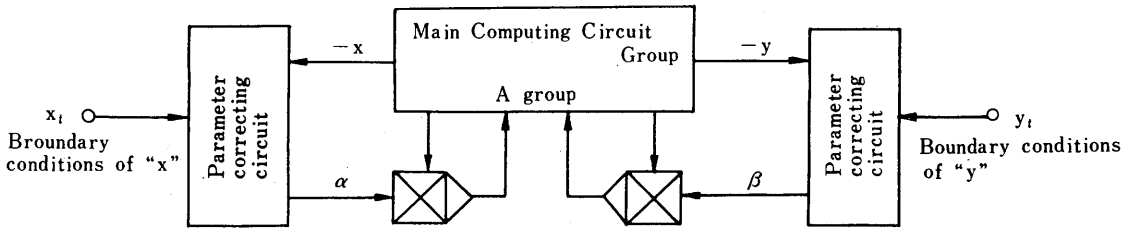


Fig. 2.18 Logic Circuit for Analysis of Double Boundary Value Equation

2.5 Logic circuit for analysis of extreme value equation

Ordinarily, the logic circuit used in obtaining an extreme value of evaluating function "F" for an unknown parameter is more complicated than that for the boundary value equation. Fig. 2.19 indicates the principle of analysis when the number of unknown parameters is one.

First of all, evaluating function "F" (αn) pertaining to any desirable value "αn" of "α" is obtained and memorized once through the 1st trial. Next, evaluating function F ($\alpha n + \Delta\alpha$) pertaining to $\alpha n + \Delta\alpha$ is obtained, and this function is compared with the previously memorized function F (αn).
When F ($\alpha n + \Delta\alpha$) - F (αn) >0, the value of α is corrected to the direction in which the value is reduced from the trial value αn through the 1st trial in proportional to $|F(\alpha n+\Delta\alpha) - F(\alpha n)|$, and when F ($\alpha n+\Delta\alpha$) - F ($\alpha n$) <0, the value of α is corrected to the direction in which the value is increased from αn in proportional to $|F(\alpha n + \Delta\alpha) - F(\alpha n)|$.
When the value of corrected α is $\alpha n + 1$, the above operation is repeated during the 2nd trial, using $\alpha n + 1$ as the starting point. In this manner, the converged value αm is obtained. However, it should be noted that the value of α may vibrate when the value of α enters the range of $\alpha m \pm \Delta\alpha$. In this case, it is recommended to reduce the value of $\Delta\alpha$ slightly at the final step of convergence.

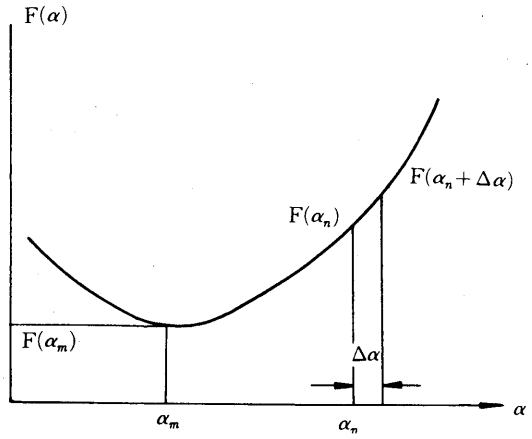


Fig. 2.19 Extreme Value Equation Analysis Principle

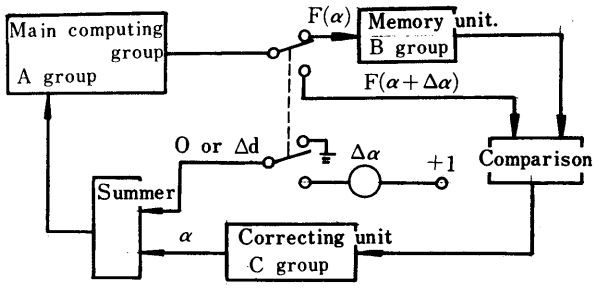


Fig. 2.20 Principle Diagram of Extreme Value Equation Analysis

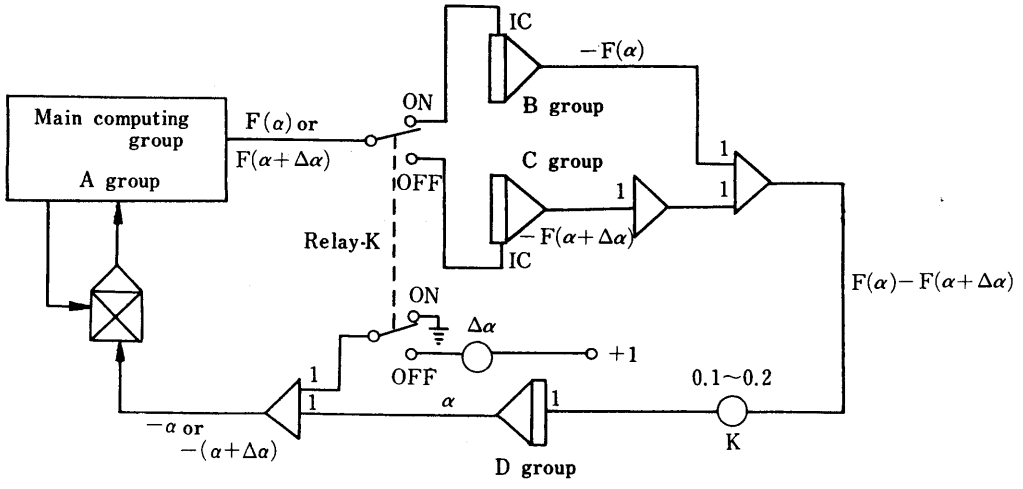


Fig. 2.21 Logic Circuit for Extreme Value Equation Analysis (1)

	t_1	t_2	t_3	t_1	t_2	t_3
A group	RESET	COMP	HOLD	RESET	COMP	HOLD
B group	HOLD	RESET	HOLD	HOLD	HOLD	HOLD
C group	HOLD	HOLD	HOLD	HOLD	RESET	HOLD
D group	COMP	HOLD	HOLD	HOLD	HOLD	HOLD
Relay K	ON	ON	ON	OFF	OFF	OFF

Fig. 2.22 Logic Control Modes

Fig. 2.21 is a circuit diagram of the flow chart shown in Fig. 2.20 expressed more practically. The control mode is shown in Fig. 2.22. For relay K used in this circuit is of a comparator which is driven by the flip-flop output of the logic patch board. Individual integrators of the B, C, and D groups are directly controlled from the logic patch board as shown in Fig. 2.25. The practical connecting method on the patch board is shown in Fig. 2.23.

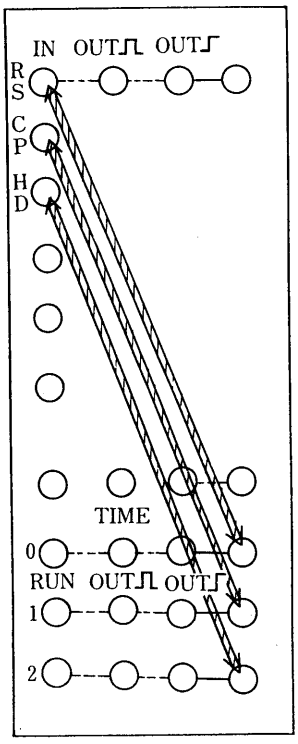


Fig. 2.23 Control Mode Connection Diagram

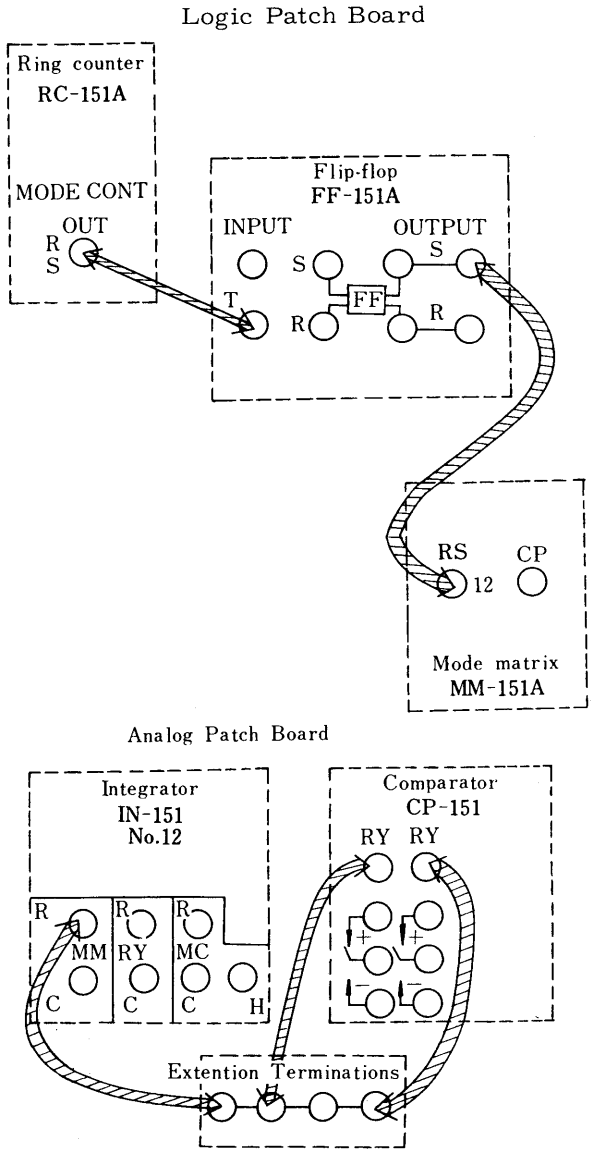
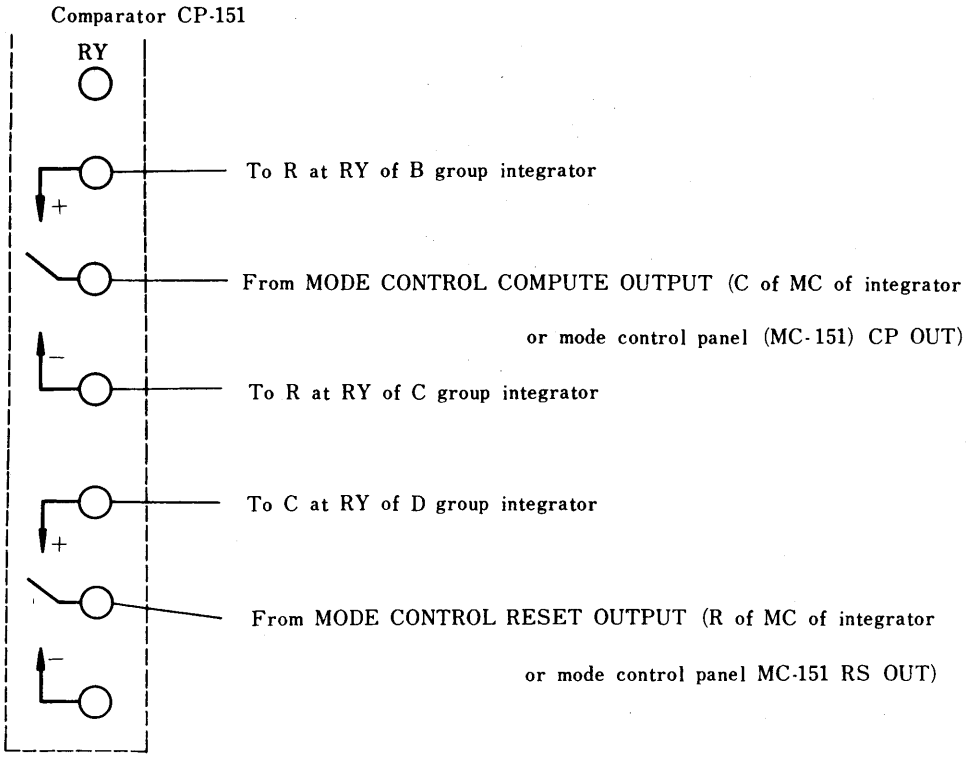


Fig. 2.24

Note: Terminal RS of No. 12 on the mode matrix (MM-151A) is interconnected to R of MM of the integrator (IN-151) No. 12.

Comparator CP-151



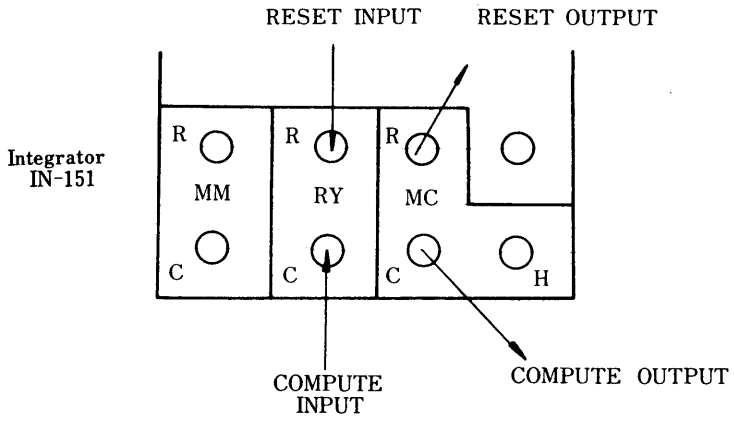


Fig. 2.25 B, C, and D Group Operation Control

For all methods to resolve the extreme value described above, the number of unknown parameters is one. Also, in the case of a multiple number of unknown parameters, the basic idea is the same. For example, consider a case in which two unknown parameters are involved. Assuming that the two variables are α and β, and that the evaluating function decided by the variations is F (α and β), upon obtaining the most suitable values (αm and βm) after starting from points (α_0 and β_0), the minor change $\triangle$F of F against the minor changes of $\triangle\alpha$ and $\triangle\beta$ is expressed by the following equation:

$$F = \frac{\partial F}{\partial \alpha}\triangle\alpha + \frac{\partial F}{\partial \beta}\triangle\beta$$

Thus, the evaluations against $\triangle\alpha$ and $\triangle\beta$ are determined as follows:

$$(\triangle\alpha)_0 = -K\frac{\partial F}{\partial \alpha} \qquad (\triangle\beta)_0 = -K\frac{\partial F}{\partial \beta}$$

and α_1 and β_1 are decided so that the following equations are satisfied:

$$\alpha_1 = \alpha_0 + (\triangle\alpha)_0$$

$$\beta_1 = \beta_0 + (\triangle\beta)_0$$

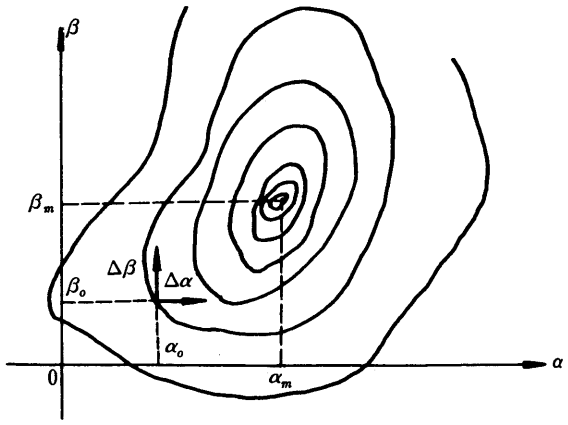


Fig. 2.26 Parameter Plane

When this calculation is performed by an analogue computer, the evaluating function F (α_0 and β_0) against the present (α_0 and β_0) is obtained. Thus, the following equations can be obtained by measuring points (α_x and β_0) which are extremely near to (α_0 and β_0) and the evaluating functions F (α_x and β_0) and F (α_0 and β_x) at (α_0 and β_x):

$$\frac{F(\alpha_x, \beta_0) - F(\alpha_0, \beta_0)}{\alpha_x - \alpha_0} = \left(\frac{\partial F}{\partial \alpha}\right)_{\alpha_0, \beta_0}$$

$$\frac{F(\alpha_0, \beta_x) - F(\alpha_0, \beta_0)}{\beta_x - \beta_0} = \left(\frac{\partial F}{\partial \beta}\right)_{\alpha_0, \beta_0}$$

where, $\left\{ \begin{array}{l} \alpha_x - \alpha_0 = \triangle\alpha \\ \beta_x - \beta_0 = \triangle\beta \end{array} \right\}$

Position of (α_1 , β_1) which are much nearer to the most suitable points than (α_0 , β_0) are determined as follows:

$$\alpha_1 = \alpha_0 - k\left(\frac{\partial F}{\partial \alpha}\right)_{\alpha_0, \beta_0} \qquad \beta_1 = \beta_0 - k\left(\frac{\partial F}{\partial \beta}\right)_{\alpha_0, \beta_0}$$

This method is called the Steepest Descent method.
"K" is a positive constant, and the value may be set freely. Ordinarily, however, it is better to take a large value as much as possible since the approximating speeds of α and β are increased or decreased by the value size, and to increase the approximating speed. If this value is excessively large, vibration may occur at a point near the most suitable point; thus, ordinarily, the value of "K" is reduced as the (α , β) approaches the most suitable point.

Now, considering an equation in which a 2-variable high-dimension algebraic equation is solved within the range of a real quantity based on the above-described theories for the example, let us attempt to compose a logic circuit of the analogue computer.
Assuming the given equations to be:

$$G(x, y) = 0 \qquad H(x, y) = 0$$

and the evaluating function to be:

$$F = |G(x, y)| + |H(x, y)|$$

the logic circuit to obtain the values of x and y so that F becomes zero can be illustrated as follows.

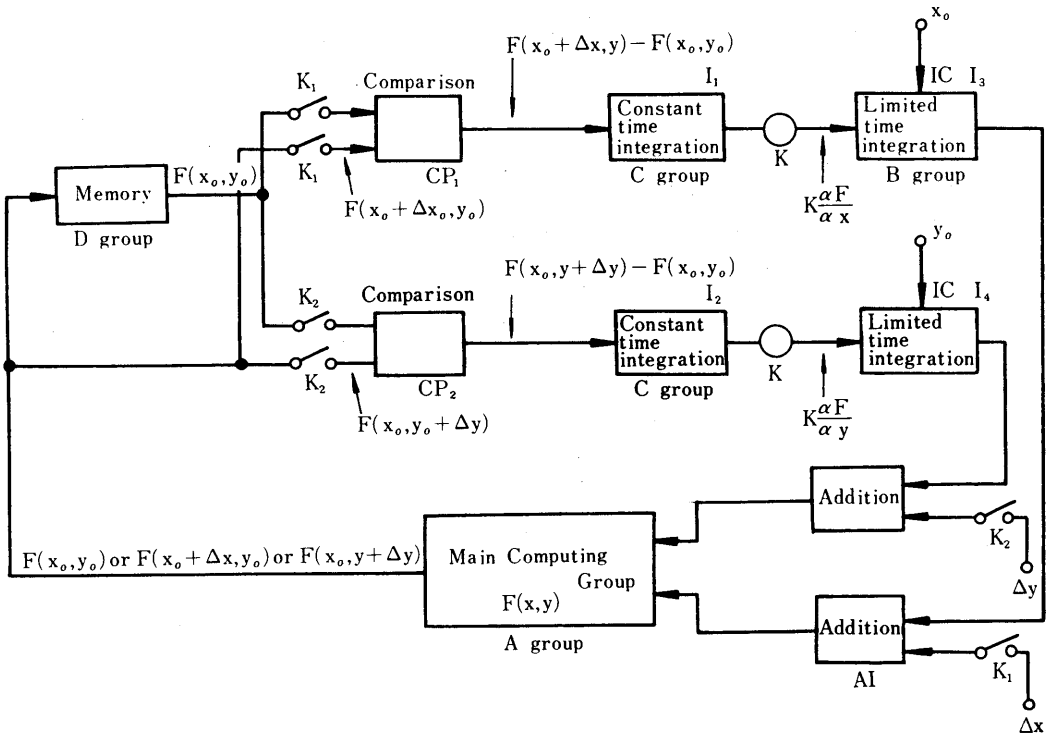


Fig. 2.27 Extreme Value Equation Analysis Block Diagram by the Steepest Descent Method

First of all, with both relay contacts K_1 and K_2 set to OFF, the 1st starting points (x_0, y_0) are applied to the main computing group through summers A1 and A2 (the values of x_0 and y_0 may be set arbitrarily. In the main computing group, F (x_0, y_0) is prepared, and the value is memorized once in the memory element of the D group. Next, relay contact K_1 is set to ON, $x_0 + y$, y_0 are applied to the main computing unit in lieu of the $x_0 \cdot y_0$, and F ($x_0 + x$, y_0) is obtained at the output.
The relay K_1 has been set to ON; thus, the previously memorized F ($x_0 \cdot y_0$) and the F ($x_0 + x, y_0$) are applied to the comparing element CP_1 simultaneously, and the differential is integrated by limited time integrator I_1 of C group. As a result, the following voltage is induced on the limited time integrator I_1 of the C group:

$$k\left(\frac{\partial F}{\partial x}\right)_{x_0,\, y_0}$$

Next, when K_1 is set to OFF, and simultaneously K_2 is set to ON, $K\,(\partial F/\partial y)_{x_0 \cdot y_0}$ is induced on the limited time integrator I_2 of the C group.

Now, voltages $K\,(\partial F/\partial x)_{x_0 \cdot y_0}$ and $K\,(\partial F/\partial y)_{x_0 \cdot y_0}$ induced on the I_1 and I_2 are integrated by I_3 and I_4 respectively, and $x_0 + K\,(\partial F/\partial x)_{x_0 \cdot y_0}$ and $y_0 + K\,(\partial F/\partial y)_{x_0 \cdot y_0}$ respectively are obtained at the outputs. These values must be closer to the optimized values than $x_0 \cdot y_0$ described previously.

When the above operations are repeated, based on the equations in the following calculations, the values of x and y are approximated gradually to the optimized values x_m and y_m.

$$x_1 = x_0 + K\left(\frac{\partial F}{\partial x}\right)_{x_0,\, y_0}$$

$$y_1 = y_0 + K\left(\frac{\partial F}{\partial y}\right)_{x_0,\, y_0}$$

However, when the dimension of an algebraic equation becomes high, the quantity of roots which satisfy the equation naturally becomes multiple. For this reason, the approximating values of x and y vary, depending on how the initial xo and yo are given. Thus, if those roots are needed, the vicinity of figures where the roots are assumed to exist must be completely sought for.

Now, when Fig. 2.27 is composed in a practical logic circuit, it becomes as shown in Fig. 2.29.

In this, the A group -- the main computing group of Fig. 2.27 -- does not include an integrator because the algebraic equation is taken as the example. Thus, it may be considered that the main computing group constantly performs the calculation regardless of the reset, compute, and hold.

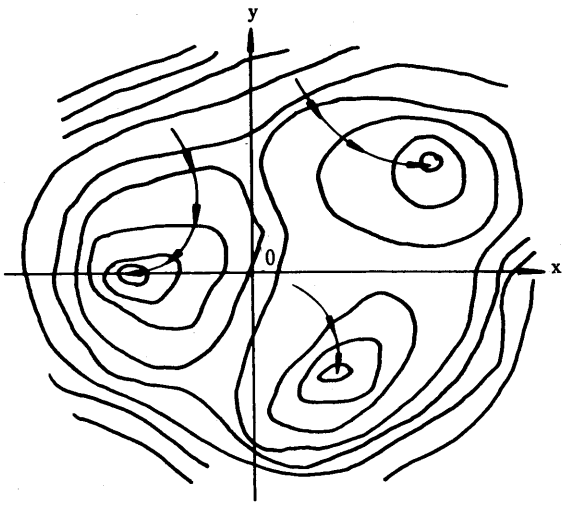


Fig. 2.28 Parameter plane

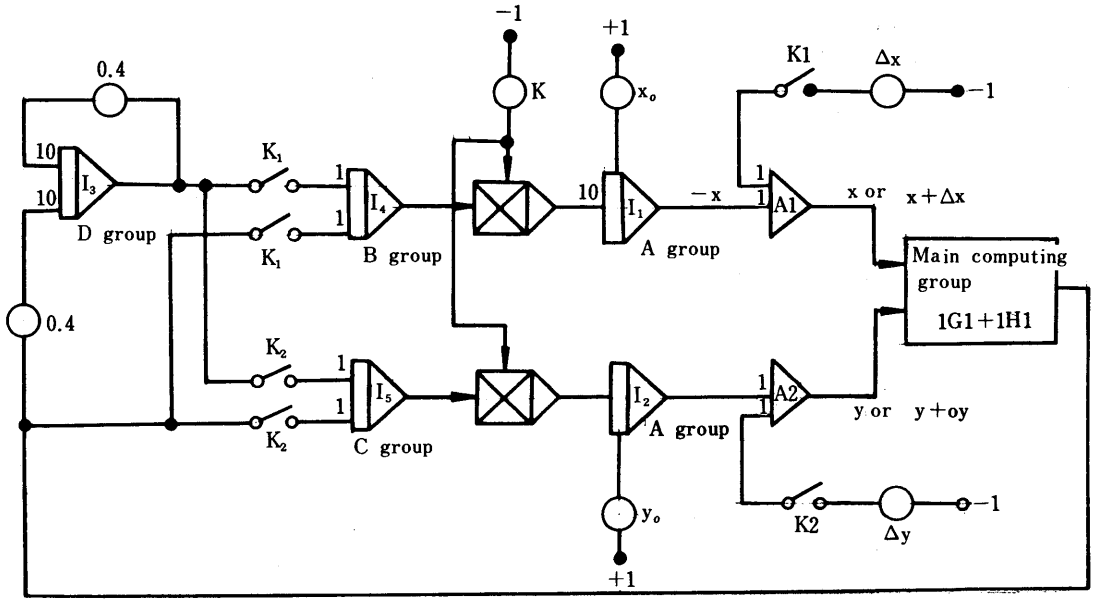


Fig. 2.29 Logic Circuit for Analysis of Extreme Value Equation

Ring counter output	1	2	3	0
A group	COMP	HOLD	HOLD	HOLD
B group	HOLD	RESET	COMP	HOLD
C group	HOLD	RESET	HOLD	COMP
D group	HOLD	COMP	HOLD	HOLD
Relay K_1	OFF	OFF	ON	OFF
Relay K_2	OFF	OFF	OFF	ON
Mode control	RESET INPUT	--	--	--

More specifically, it initially becomes as follows:

A group: RESET to COMP
B group: RESET to HOLD
C group: RESET to HOLD
D group: RESET to HOLD

Operation is started with the entire integrators I_1 through I_5 set to RESET, and by depressing the RUN push button on the logic control panel, the ring counter (in which a ring counter connection of four conditions is made) moves as 1, 2, 3, 0, 1, 2, 3, and 0 in accordance with the clock time connected to the shift input.

Integrators I_1 and I_2 of the A group start from the initial conditions x_0 and y_0, and become COMP. However, outputs of the I_1 and I_2 respectively are set stationarily on $-x_0$ and $-y_0$ since the outputs of the integrators I_4 and I_5 of the C group still remain zero.

Next, when the rated time is elapsed, and the ring counter moves to ring counter output No. 2, outputs $-x_0$ and $-y_0$ of I_1 and I_2 are stationarily set as they are and applied to the main computing group, and $|G(x_0, y_0)| + |H(x_0, y_0)|$ can be obtained at the outputs. When these values are applied to integrator I_3 of the D group, $|G(x_0, y_0)| - |H(x_0, y_0)|$ is induced at the output of I_3, since I_3 is a primarily delayed circuit with gain 1. Next, when the ring counter output moves to No. 3, $x_0 + x$, y_0 is applied to the main computing group through A_1 and A_2, because relay K_1 is set to ON as soon as the output of I_3 is held, and $G(x_0 + \triangle x, y_0) + H(x_0 + \triangle x, y_0)$ can be obtained on the output. $|G(x_0 + \triangle x, y_0)| + |H(x_0 + \triangle x, y_0)| - |G(x_0, y_0)| - |H(x_0, y_0)|$ is applied to integrator I_4 since relay K is set to ON and when this is integrated for a certain time, $k(\partial F/\partial x)_{x_0 \cdot y_0}$ has been obtained on output of the I_4. (Where, k: Constant; $F = F(x_0, y_0) = G(x, y) + H(x, y)$

Next, when the ring counter output moves to No. 0, $k(\partial F/\partial y)_{x_0 \cdot y_0}$ is obtained at output of I_5 in the manner identical to the above.

Accordingly, when the ring counter output becomes No. 1 again, I_1 and I_2 respectively integrate $k(\partial F/\partial x)_{x_0 \cdot y_0}$ and $k(\partial F/\partial x)_{x_0 \cdot y_0}$, and the following are obtained at the outputs:

$$-x_1 = -x_0 - k\left(\frac{\partial F}{\partial x}\right)_{x_0, y_0} \qquad -y_1 = -y_0 - k\left(\frac{\partial F}{\partial y}\right)_{x_0, y_0}$$

When the above calculations are repeated, based on the values x and y, optimized values x_1 and y_1 of the x and y are obtainable.

An example of a logic circuit for analysis of a 5-parameter extreme value problem is indicated in the following diagram as an example of logic circuit for analysis of an ordinary multi-extreme value equation. This block diagram has been composed for analysis of a 5-element, simultaneous, high-dimensional equation.

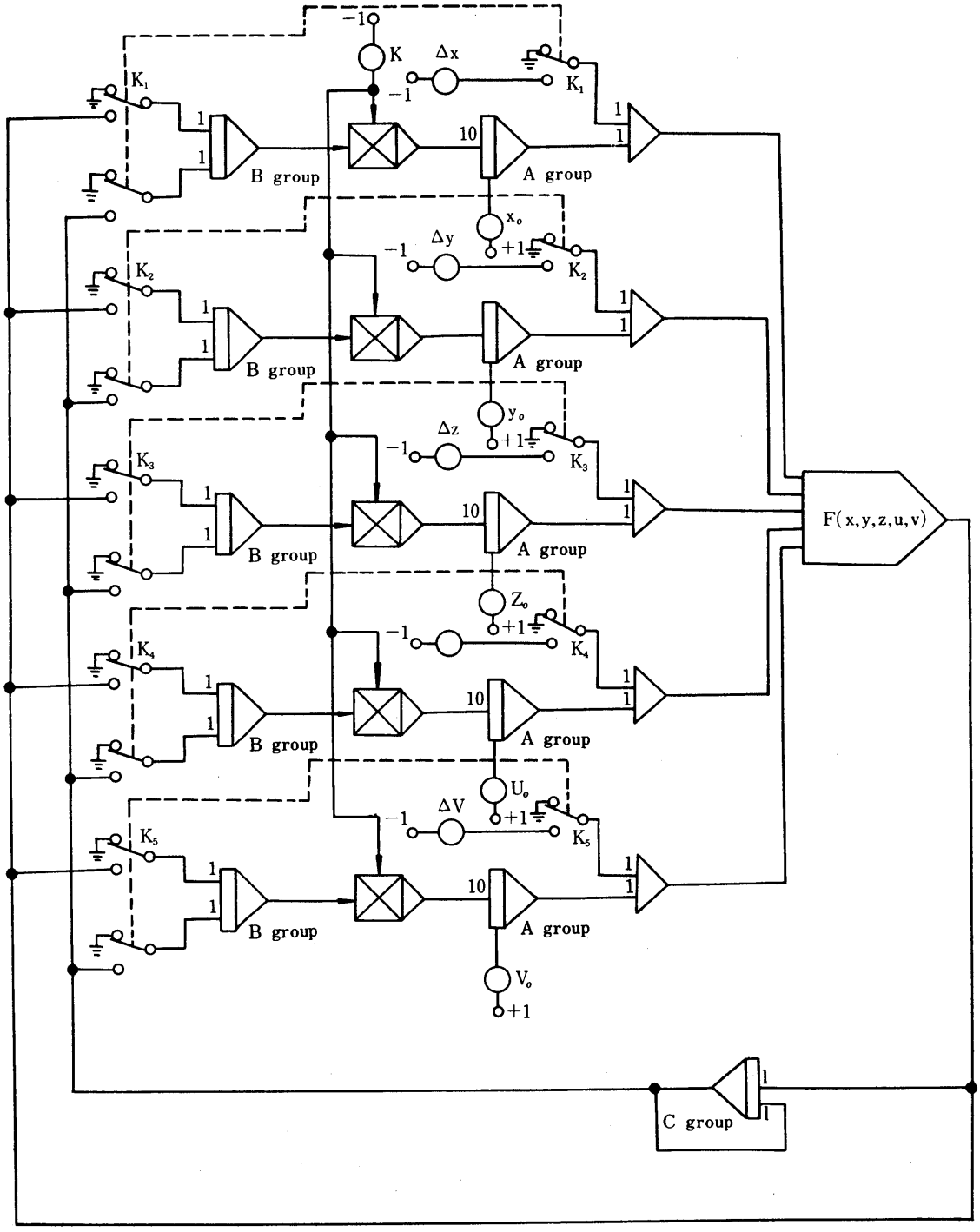


Fig. 2.30 Logic Circuit for Analysis of 5-element, Simultaneous, High-dimensional Algebraic Equation

Equations solved by this circuit diagram are as follows:

$G_1(x, y, z, u, v) = 0$

$G_2(x, y, \ldots . v) = 0$

. . . . . .

$G_5(x, y, z, u, v) = 0$

Where, the evaluating function is decided as follows:

$$F(x, y, z, u, v) = |G_1| + |G_2| + |G_3| + |G_4| + |G_5|$$

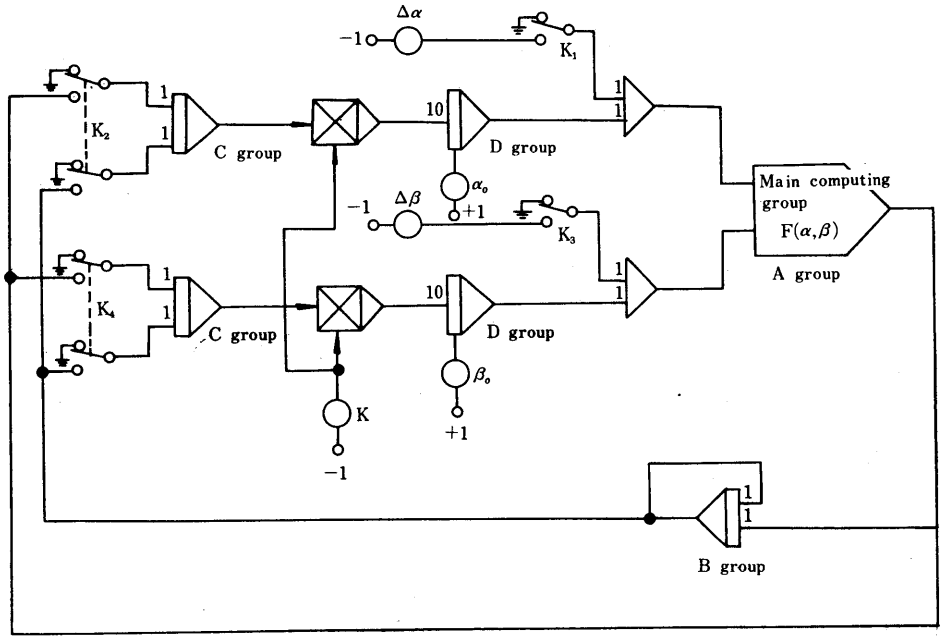
The circuit of Fig. 2.30 is intended to obtain the values of x, y, zu, u, and v so that the F becomes zero. The operation modes to drive this circuit are indicated in Fig. 2.31.

Computation is started by setting the LOGIC CONTROL on the logic control panel to RUN.

Ring counter output		1	2	3	4	5	6	0
A group	R	C	H	H	H	H	H	H
B group	R	H	R	C	C	C	C	C
C group	R	H	C	H	H	H	H	H
Relay K_1				ON				
Relay K_2					ON			
Relay K_3						ON		
Relay K_4							ON	
Relay K_5								ON
Mode control panel	ALL RESET	RESET	--	--	--	--	--	--

Fig. 2.31 Operational Control Mode

In the logic circuit for analysis of the 5-variable, extreme value equations described above, the main computing group may not include an integrator. When the main computing group includes an integrator, the circuit composition somewhat differs. The following diagram shows an example of a logic circuit for analyzing 2-variable, extreme value problem (This is not an algebraic equation).

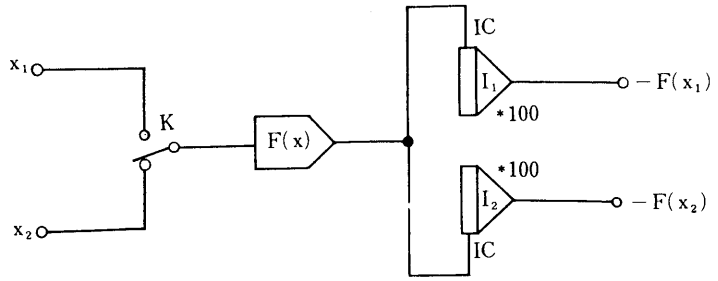


Ring counter output	1	2	3	4	5	6	7	8	0
A group	R	C	H	R	C	H	R	C	H
B group	R	R	C	H	H	H	H	H	H
C group	H	R	R	R	R	C	H	H	C
D group	C	H	H	H	H	H	H	H	H
Relay K_1	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
Relay K_2									
Relay K_3	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
Relay K_4									ON

Fig. 2.32 Logic Circuit for Analysis of 2-variable, Extreme Value Problem

2.6 Time Sharing Operation

Time sharing operation is defined as a computing system in which an electronic system function generator is used by dividing with the time band, and elements of one unit are utilized instead of using several same units. The circuit consists of relay elements, sample hold element (memory element), and electronic multiplier or function generator, and the output waveform is approximated with an echelon-shaped waveform.



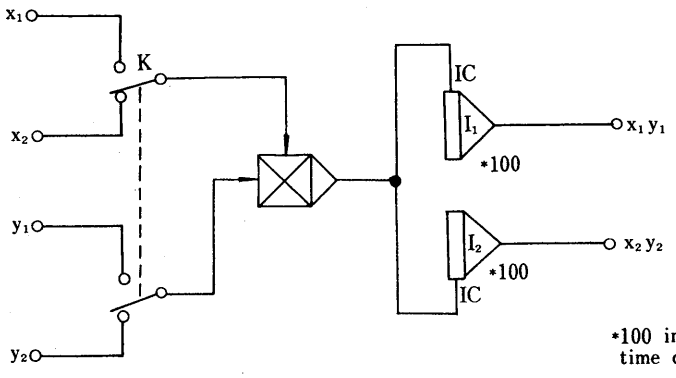
*100 indicates that the integrating time constant is 100.

Relay K indicates that the relay is set to OFF.

Fig. 2.33 Time Sharing Operation Circuit Diagram (When a function generator)

The relay contact of Fig. 2.33 repeats ON-OFF operations with 10 c/s (100 ms). Moreover, the relation between integrators #1 and #2 and relay K should be as follows:

Relay K	ON	OFF
Integrator 1	RESET	HOLD
Integrator 2	HOLD	RESET



*100 indicates that the integrating time constant is 100.

Fig. 2.34 Time Sharing Operation Circuit (When a multiplier)

The above two examples utilize elements of one unit for two units. When utilizing for three or more units, a circuit utilizing ring counter is constructed.

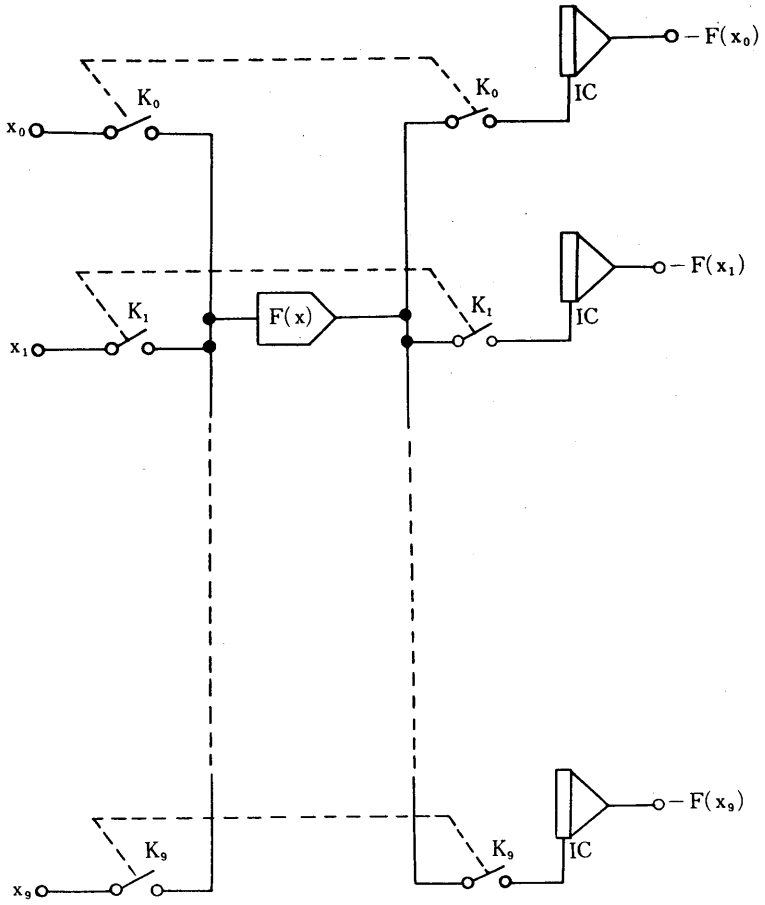


Fig. 2-35 Time sharing operation.

Relay \ Ring counter	0	1	2	. . . .	9
k_0	ON				
k_1		ON			
k_2			ON		
. . . . .				. . . .	
k_9					ON

Integrator In is reset when relay Kn is set to ON.
The integrator is held except when relay Kn is set to ON.

3. Exercises for Automatic Programing

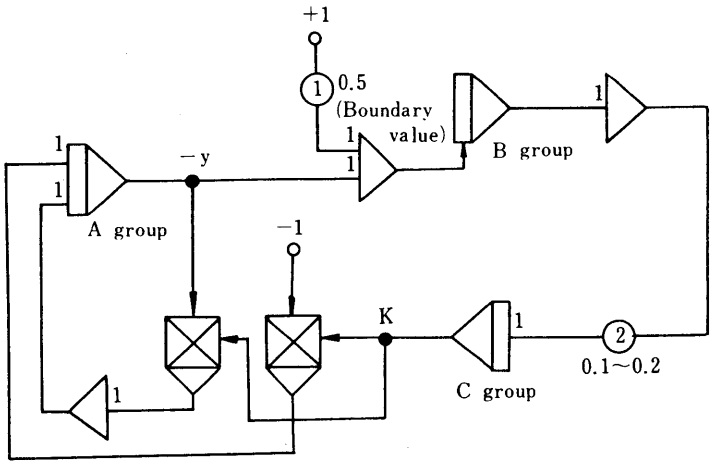
3.1 Equation of boundary value

Exercise (1)

Decide value of K at the following equation so that "y" becomes zero when "t" = 0, and "y" becomes 0.5 when "t" = 7 seconds:

$$\frac{dy}{dt} + Ky = KF(t) \qquad F(t) = 1$$

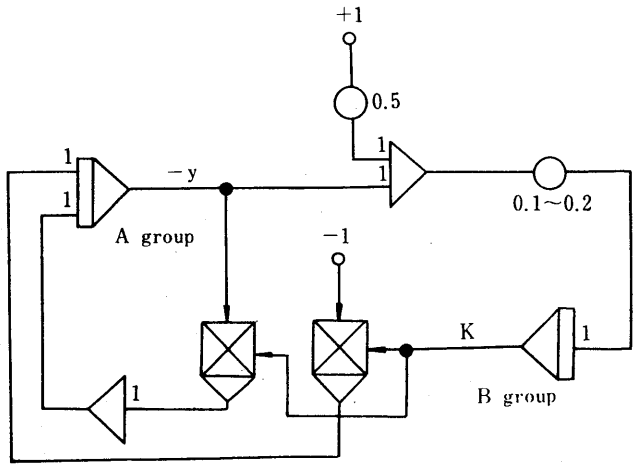
Solution (1):



	△t	7 sec
A group	B	C
B group	H	R
C group	C	H

Fig. 3.1 Exercise (1) Block Diagram

◉ Observing the movement of K, adjust the converging speed with Pot-2.



	1.5 sec	7 sec	1.5 sec
A group	R	C	H
B group	H	H	C

Fig. 3.2 Exercise (1) Block Diagram

Exercise (2)

Decide the value of "a" at the following equation so that "y" becomes 0, and "y'" becomes 0.5, when "t" is zero; and "y" becomes 0.5 when "t" is 10 seconds.

$$\frac{d^2y}{dt^2} + ay = 0$$

Solution (1)

	△t	10 sec.	△t
A group	R	C	H
B group	H	H	C

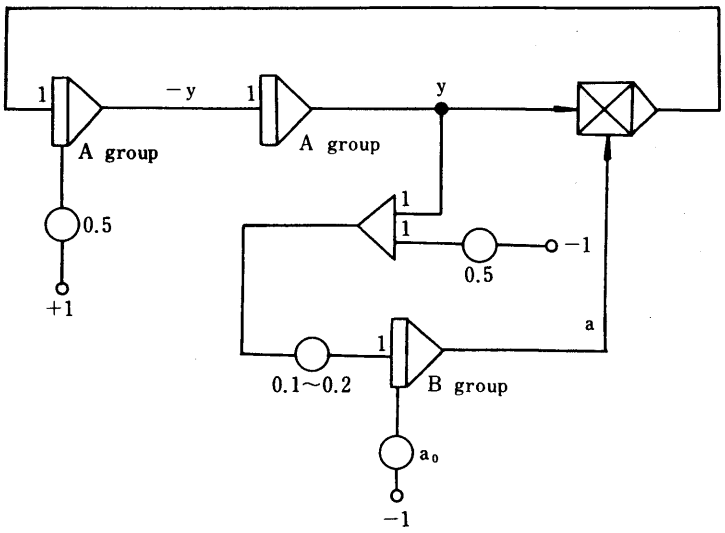


Fig. 3.3 Exercise (2) Block Diagram

Solution (2)

	△t	10 sec.	△t
A group	R	C	H
B group	H	H	C

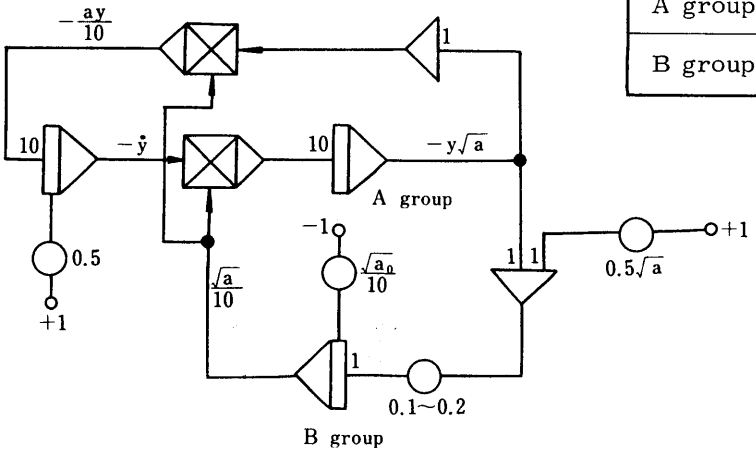


Fig. 3.4 Exercise (2) Block Diagram

Exercise (3)

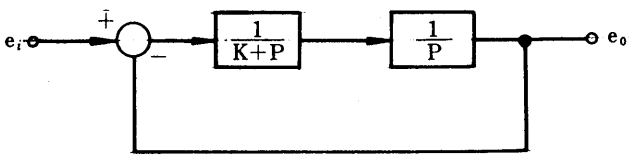


Fig. 3.5

In Fig. 3.5, decide the value of K so that the overshoot of "e_o" against step "ei" becomes 10% of the "ei".

Solution (1):

In this system, the response waveform for the step input becomes as shown by e in Fig. 3.6. Thus, when solving this equation such a logic circuit must be developed that 1.1 "ei" and maximum value of "e_o" are compared each other. Subsequently, the maximum value hold circuit described in Fig. 2.5, will employed in this logic operation.

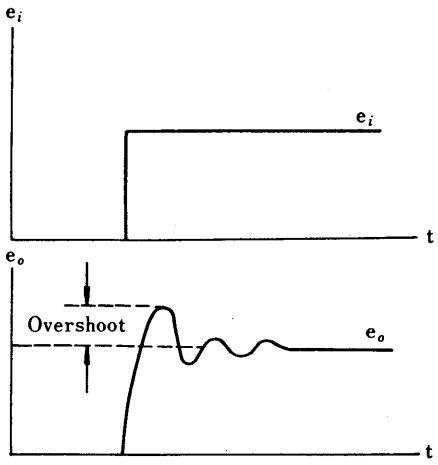


Fig. 3.6 Step Response

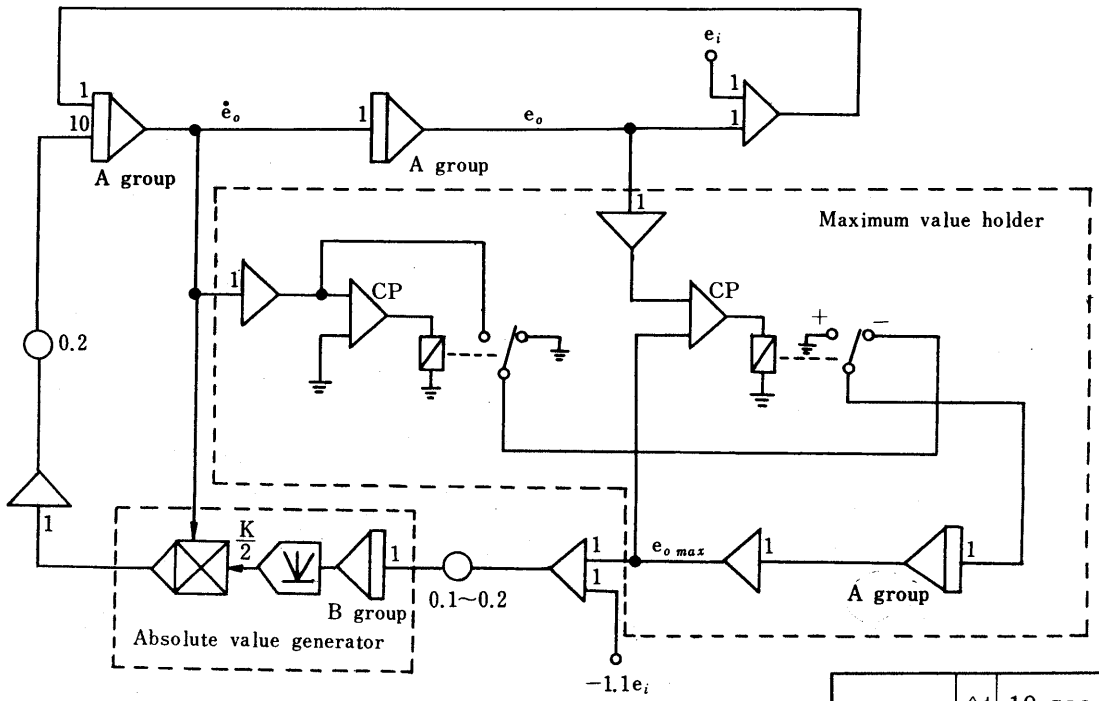
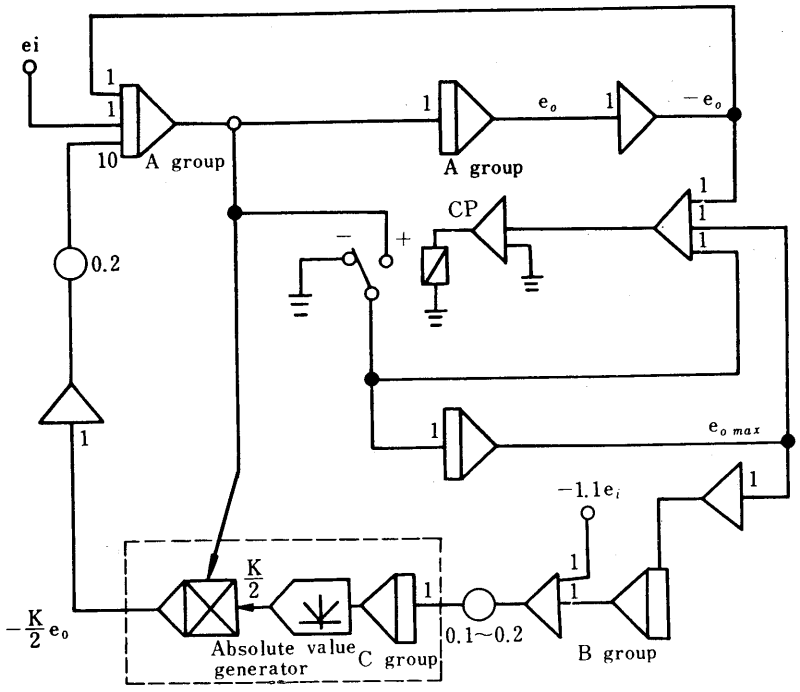


Fig. 3.7 Exercise (3) Block Diagram

	△t	10 sec.	△t
A group	R	C	H
B group	H	H	C

Note: It is proper to make "ei" be 0.5.

Solution (2):



	△t	10 sec.
A	R	C
B	H	R
C	C	H

Fig. 3.8 Exercise (3) Block Diagram

Exercise (4)

Decide the values of $x_0 = (dx/dt)_{t=0}$ and $y_0 = (dy/dt)_{t=0}$ at the following equations so that "x" becomes 1, and "y" becomes zero, when "t" is zero; and "x" becomes zero, and "y" becomes "1", when "t" is 5 seconds.

$$\frac{d^2x}{dt^2} = xy \qquad \frac{d^2y}{dt^2} = xy$$

Solution:

When the equation satisfies the boundary conditions, the solution will become as shown in Fig. 3.9. Therefore, assuming that x and y at t = 5 are dependent to x_0 and y_0 respectively and also assuming that there is no mutual relation between these parameters, the block diagram becomes as shown in Fig. 3.10.

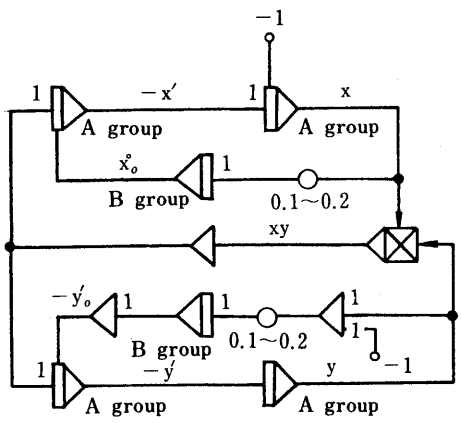


Fig. 3.10 Exercise (4) Block Diagram

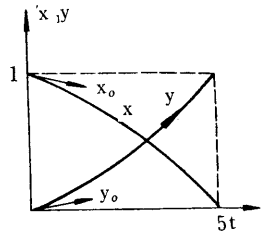


Fig. 3.9

	△t	5 sec	△t
A	R	C	H
B	H	H	C

Exercise (5)

Decide the values of "a" and "b" so that "y" becomes "a," and "y" becomes "b," when "t" is zero; and "y" becomes "a," and "y" becomes "b," when "t" is 2 in the following equation:

$$\frac{d^2y}{dt^2} + 0.1\frac{dy}{dt} + y^3 = 0.4 \cos t$$

Solution:

When scale conversion is applied to the given equation:

$$\left[\frac{d^2y}{2dt^2}\right] = -0.1\left[\frac{dy}{2dt}\right] - 4\left[\frac{y}{2}\right]^3 + 0.2 \cos t$$

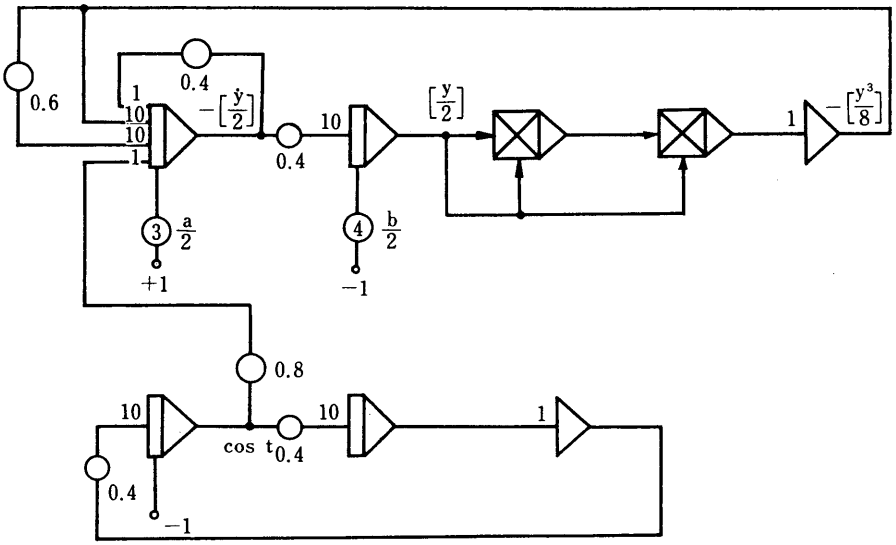


Fig. 3.11 Block Diagram in which Time Axis is Reduced to 1/4

When this block diagram is recomposed for automatic programming, it becomes as follows:

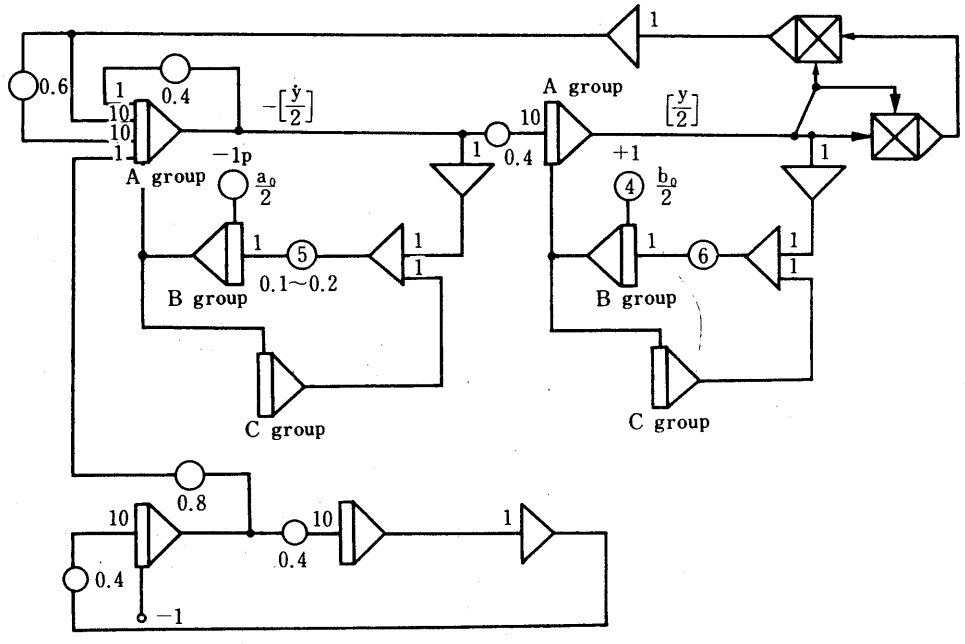


Fig. 3.12 Exercise (5) Block Diagram

In this equation, the optimized values of a and b will differ depending how the initial values of a_0 and b_0 are given. Accordingly, optimized value must be obtained by starting from all points included in $-2 \leqq a \leqq 2$ and $-2 \leqq b \leqq 2$. Actually, however, it is sufficient to obtain such values by starting from any of several desired points after properly deciding the lattice points on the a-b plane.

(1) After setting the question on the patch board, the proper values of a_0 and b_0 are applied to pot 3 and 4.

(2) Confirm that the values of pot 5 and pot 6 remain the same each other.

(3) After the completion of converging, change the a_0 and b_0 again with pot 3 and 4, and repeat the above operations.

	Δt	$\frac{2\pi}{4}$sec	Δt
A	R	C	H
B	H	H	C
C	R	H	H

Fig. 3.13 Control Signal for Driving

3.2 Extreme Value Equation

Exercise (6)

Obtain the value of K so that the control tolerance area of e_0 against step input ei becomes the minimum at the following transfer function:

$$e_0 = + \frac{1}{p^2 + KP + 1} \cdot ei$$

Solution (1):

The control tolerance area is those portions indicated by oblique lines in Fig. 3.14.

Thus, this area is obtained by calculating the following equation:

$$\int_{t_1}^{\infty} | e_0 - ei | \, dt$$

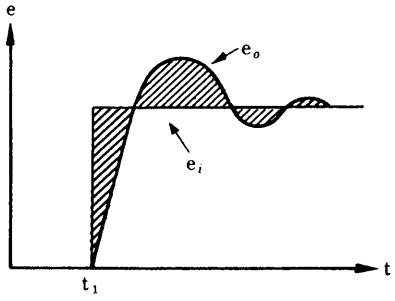


Fig. 3.14 Control Tolerance Area

The block diagram can be expressed as follows by Fig. 2.21. Moreover, Fig. 3.15 indicates the condition in which the control tolerance area changes, depending on the size of the value of K.

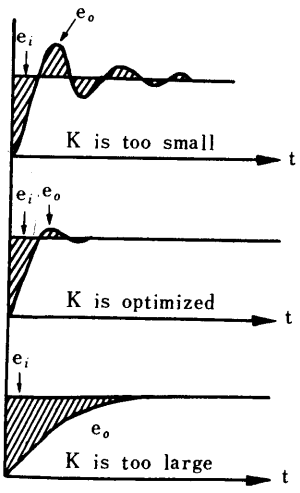


Fig. 3.15

	3 sec	10 sec	2 sec	3 sec	10 sec	2 sec
A group	R	C	H	R	C	H
B group	H	R	H	H	H	H
C group	H	H	H	H	R	H
D group	C	H	H	H	H	H
Relay K	ON	ON	ON	OFF	OFF	OFF

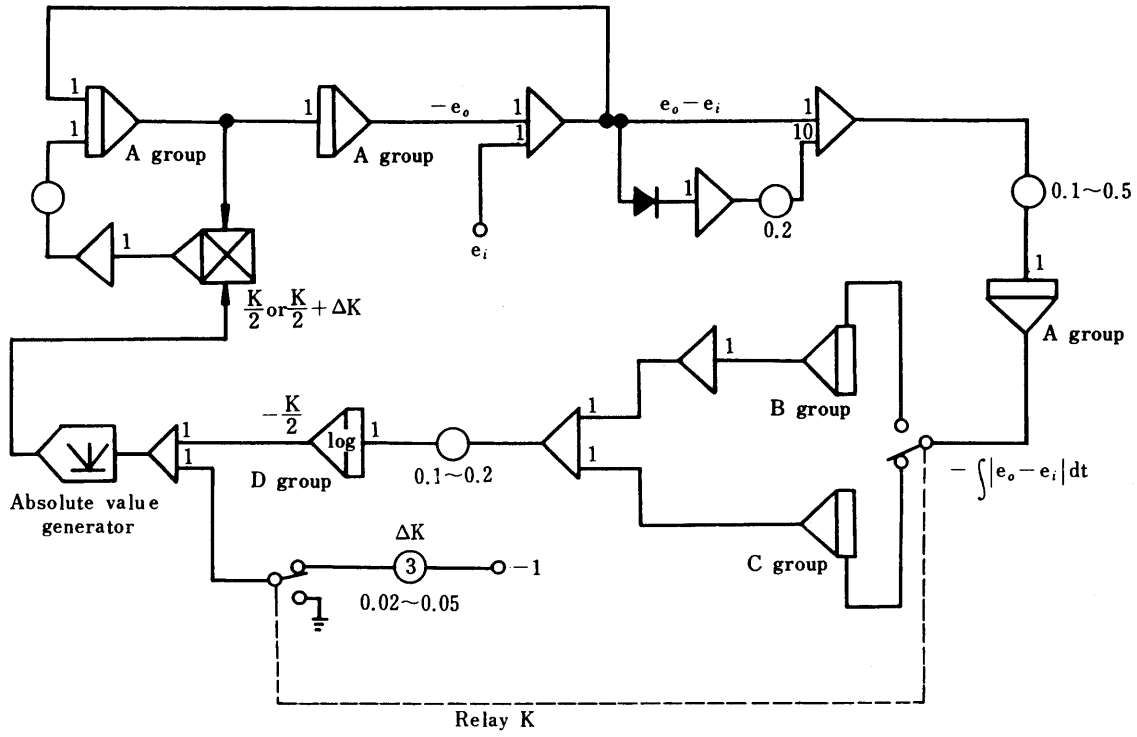


Fig. 3.16 Exercise (6) Block Diagram

(1) When the value of K approaches the optimized value (km), reduce the value of Pot 3 as much as possible. 0.02 would be suitable.

If reduced excessively, an error may occur in the optimized value.

(2) The value of obtaining K can be approximately expressed as follows when the approaching value of I_{08} is assumed to be -Kn/2:

$$\frac{kn}{2} = \frac{1}{2}\left\{\frac{Kn}{2} + \left(\frac{Kn}{2} + \Delta K\right)\right\} = \frac{1}{2}(Kn + \Delta K)$$

Solution (2):

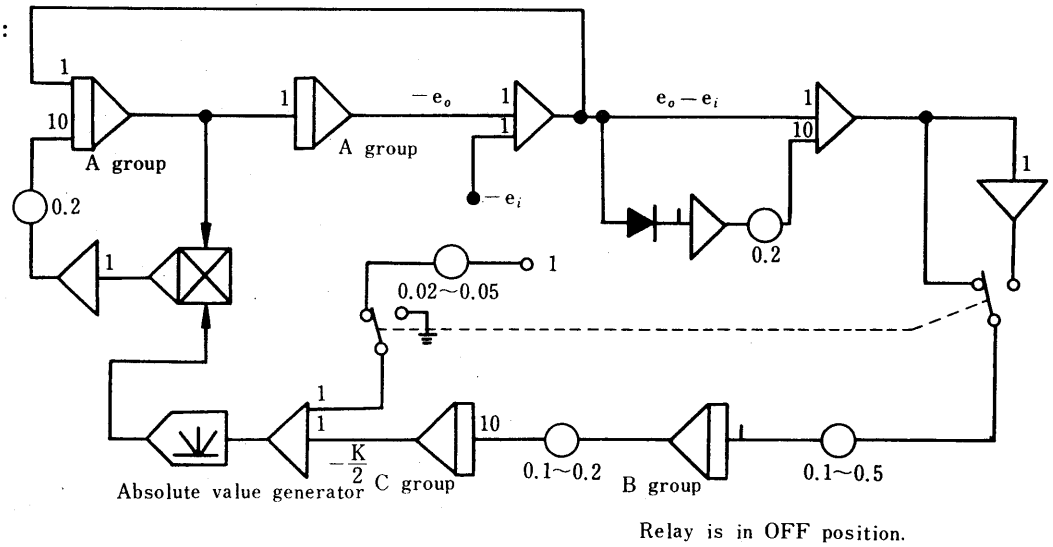


Fig. 3.17 Exercise (6) Block Diagram

Exercise (7)

Solve the following equations:

$$\begin{cases} x^2 + y^2 - 5 = 0 \\ 3x^2 + x^3 - y^2 = 0 \end{cases}$$

Solution:

Reforming the above equations to:

$$F_1(x, y) = x^2 + y^2 - 5$$

$$F_2(x, y) = 3x^2 - x^3 - y^2$$

apply the proper values to x and y, and obtain the values of x and y so that the following equation is satisfied:

$$F(x, y) = |F_1(x, y)| + |F_2(x, y)| = 0$$

The method of solving an algebraic equation of this type by means of automatic programming was already described in section 2.5, therefore, how to compose a practical circuit is explained from here on.

As the circuit outline, it is classifiable into the following four units:

Part A: Calculates $F(x, y)$

Part B: Calculates $F(\triangle x + x, y) - F(x, y)$ $F(x, y + \triangle y) - F(x, y)$

Part C: Memorizes $F(x, y)$

Part D: Corrects values of x and y with values which are in proportion to $F(x + \triangle x, y) - F(x, y)$ and $F(x, y + \triangle y) - F(x, y)$

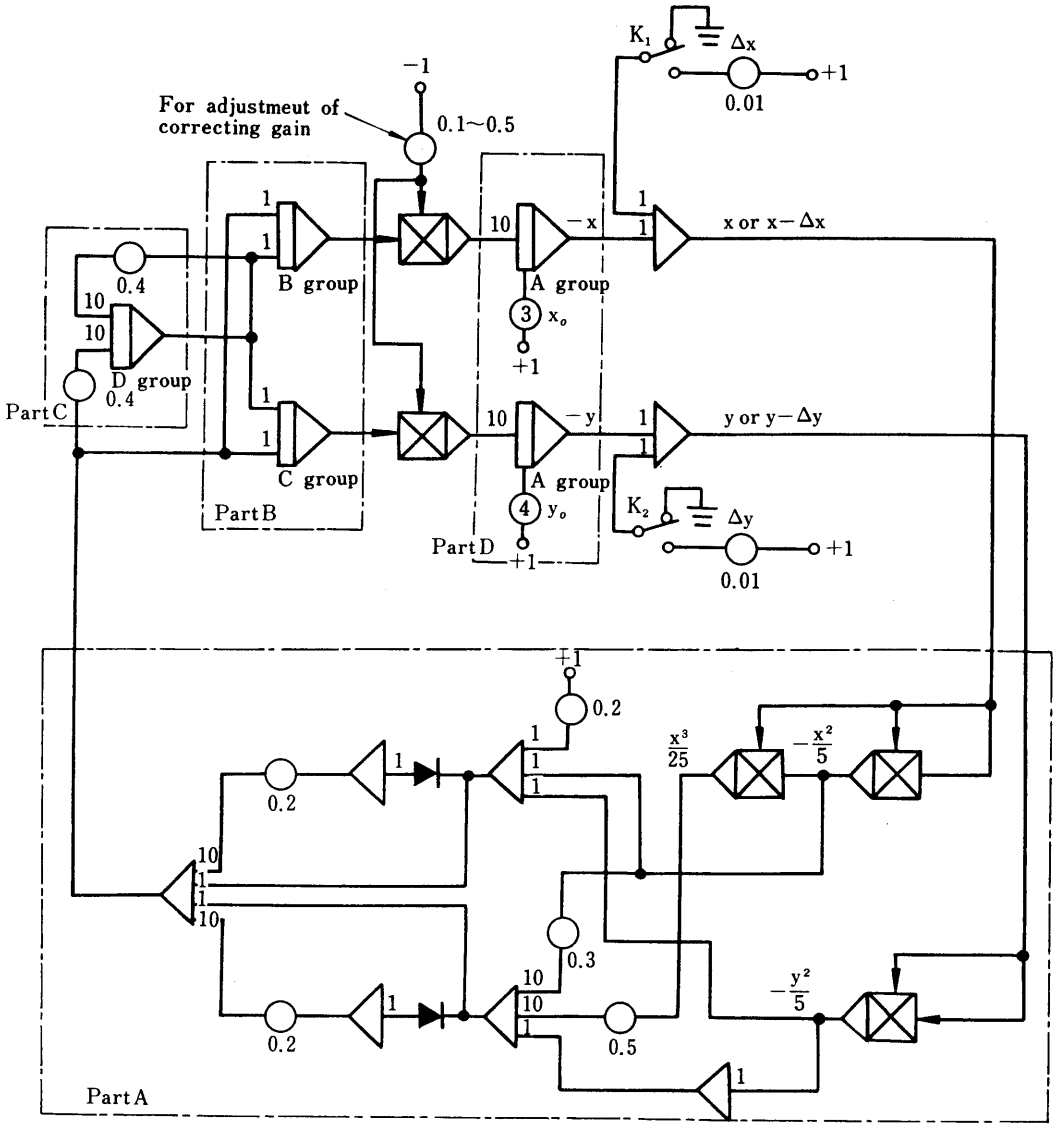


Fig. 3.18 Exercise (7) Block Diagram

100V is assumed to be 5.

When performing automatic operation control of this block diagram, use a ring counter and compose the control modes as shown in Fig. 3.19.

Conditional terminal number	1	2	3	4	0
Relay K_1	--	--	ON	--	--
Relay K_2	--	--	--	ON	--
A group	C	H	H	H	H
B group	H	R	C	H	H
C group	H	H	R	C	H
D group	R	C	H	H	H

Fig. 3.19 Logic Operation Control Modes for Exercise (7)

Upon completion of the entire programming (including that on the ring counter), set the proper X_0 and Y_0 on pot 3 and 4 of Fig. 3.18.

Exercise (8)

Solve the following equation:

$$Z^3 - 5Z^2 + 9Z - 5 = 0$$

Solution:

Assuming $Z = X + yi$, apply this to the above equation. Then the above equation will be rewritten as follows:

$$(x + yi)^3 - 5(x + yi)^2 + 9(x + yi) - 5 = 0$$

This is calculated and becomes:

$$(x^3 - 5x^2 + 9x - 3xy^2 - 5) + i(-y^3 + 3x^2y - 10xy + 9y) = 0$$

The X and Y are real quantity; consequently, the above equations are permuted to a simultaneous high-dimensional algebraic equation of the exercise (7) as follows:

$$x^3 - 5x^2 + 9x - 3xy^2 - 5 = 0$$

$$-y^3 + 3x^2y - 10xy + 9y = 0$$

3.3 Time Sharing Operation

Exercise (9)

Assume that a material has a thickness of ℓ cm, on one surface of which no heat transmission is conducted. The other surface contacts a material having a thermal capacity of ∞, and the boundary surface is always maintained under 0°C. Now, solve the following equation which expresses the heat transmission of this material.

$$\frac{\partial \theta}{\partial t} = \frac{\partial^2 \theta}{\partial x^2} + \delta e^{\theta \times \frac{1}{50}}$$

Where, t: Time (sec)

x: Distance (cm)

θ: Temperature (°C) $\quad 0 < \theta < 100$°C

∂: Coefficient of heat generation $\quad 0.10 \sim 10.0$

ℓ: 5 cm

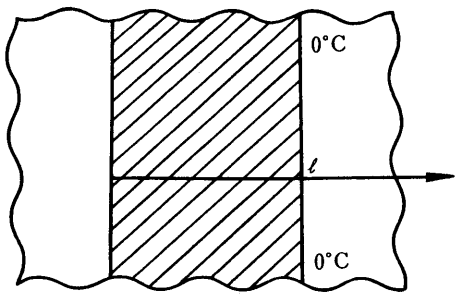


Fig. 3.20

Solution:

Dividing the material equally into five pieces (may be divided into ten pieces), and assume the temperatures of the individual surfaces to θ_0 , θ_1 , θ_2 , ... , θ_5 . Further, when width of the divided sections is assumed to be $\triangle x$, the following constant difference equations can be obtained.

$$\frac{d\theta_0}{dt} = \frac{1}{\triangle x^2}(2\theta_1 - 2\theta_0) + \delta e^{\frac{\theta_0}{50}}$$

$$\frac{d\theta_1}{dt} = \frac{1}{\triangle x^2}(\theta_2 - 2\theta_1 + \theta_0) + \delta e^{\frac{\theta_1}{50}}$$

$$\frac{d\theta_2}{dt} = \frac{1}{\triangle x^2}(\theta_3 - 2\theta_2 + \theta_1) + \delta e^{\frac{\theta_2}{50}}$$

$$\frac{d\theta_3}{dt} = \frac{1}{\triangle x^2}(\theta_4 - 2\theta_3 + \theta_2) + \delta e^{\frac{\theta_3}{50}}$$

$$\frac{d\theta_4}{dt} = \frac{1}{\triangle x^2}(\theta_5 - 2\theta_4 + \theta_3) + \delta e^{\frac{\theta_4}{50}}$$

Converting the scale of the equations, considering $\theta_5 = 0°C$, $0 < \theta < 100°C$ and $\triangle x = 1cm$, the new equation will be:

$$\frac{1}{100}\frac{d\theta_0}{dt} = 2\left(\frac{\theta_1}{100} - \frac{\theta_0}{100}\right) + \frac{\delta}{100}e^{2\times\frac{\theta_0}{100}}$$

$$\frac{1}{100}\frac{d\theta_1}{dt} = \frac{\theta_2}{100} - 2\times\frac{\theta_1}{100} + \frac{\theta_0}{100} + \frac{\delta}{100}e^{2\times\frac{\theta_1}{100}}$$

$$\frac{1}{100}\frac{d\theta_2}{dt} = \frac{\theta_3}{100} - 2\times\frac{\theta_2}{100} + \frac{\theta_1}{100} + \frac{\delta}{100}e^{2\times\frac{\theta_2}{100}}$$

$$\frac{1}{100}\frac{d\theta_3}{dt} = \frac{\theta_4}{100} - 2\times\frac{\theta_3}{100} + \frac{\theta_2}{100} + \frac{\delta}{100}e^{2\times\frac{\theta_3}{100}}$$

$$\frac{1}{100}\frac{d\theta_4}{dt} = \frac{-2\theta_4}{100} + \frac{\theta_3}{100} + \frac{\delta}{100}e^{2\times\frac{\theta_4}{100}}$$

The term $\frac{\delta}{100}e^{2\times\frac{\theta_0}{100}}$ included in these equations has exactly the same function for all from θ_0 to θ_4 . Therefore, when a block diagram for time sharing operation is prepared by using a function generator of one unit, it can be illustrated as shown on Fig. 3.23. Further, Fig. 3.21 shows coordinates required in setting the function generator, the exponential function approximated by five segments. It is recommended to set functions exactly symmetrically for the vertical axis in order to reduce the number of amplifiers, and to arrange the composition so that a wave form shown in Fig. 3.22 can be finally obtained. Fig. 3.23 is a block diagram composed by using a function generator which has been established exactly symmetrically for the vertical axis.

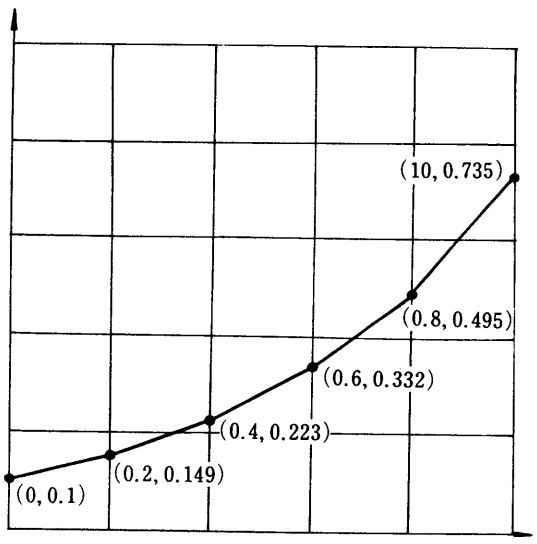


Fig. 3.21 Function Generator Setting Coordinates

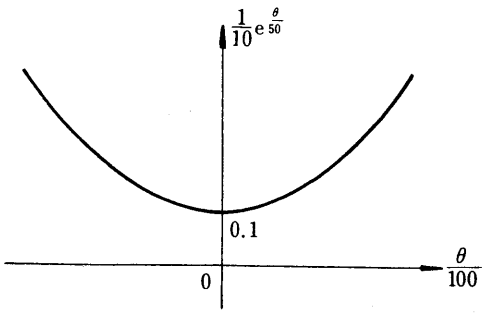
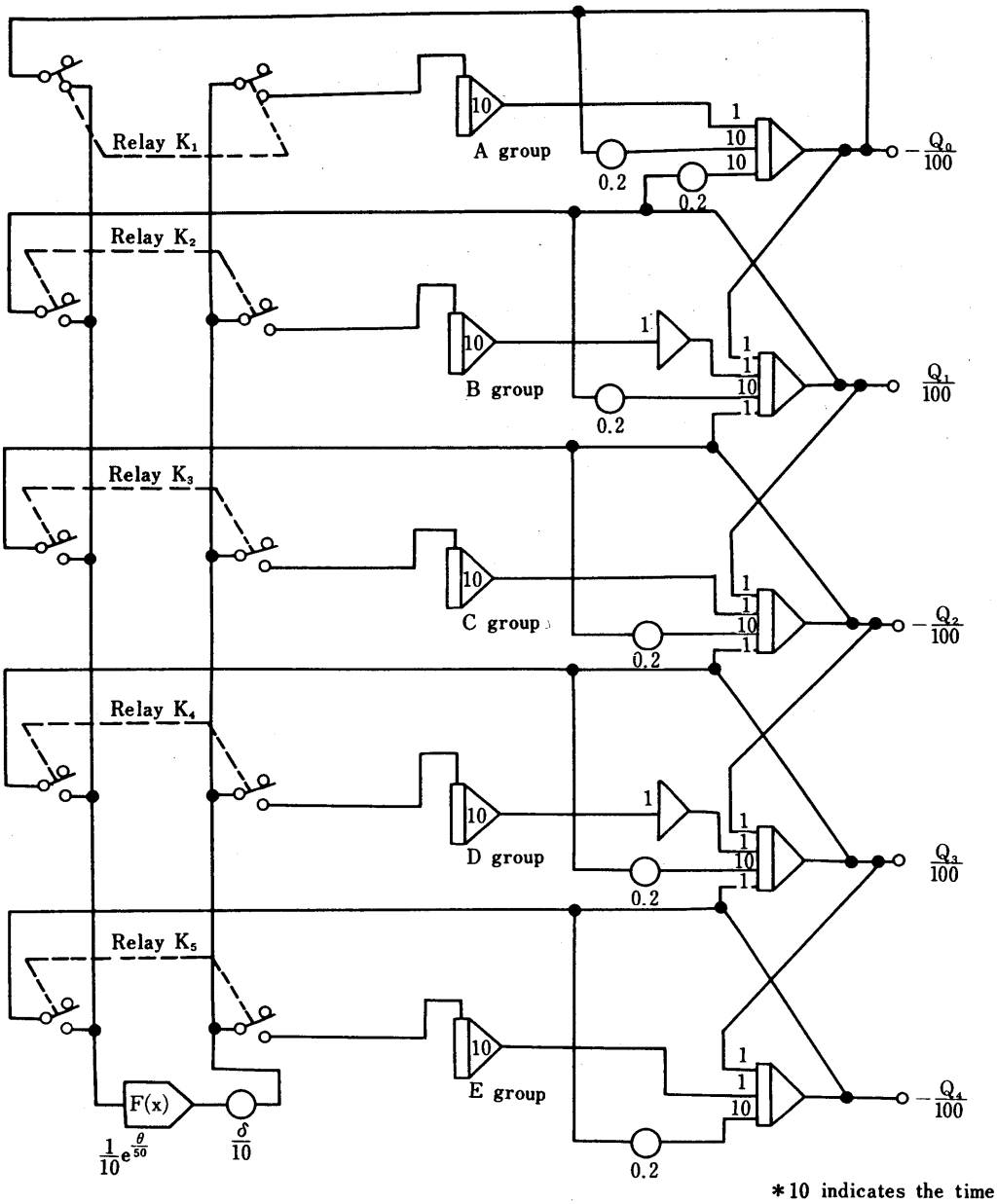


Fig. 3.22 Function Generator Setting Waveform



*10 indicates the time constant is 10.

Fig. 3.23 Exercise (9) Block Diagram

Ring counter output	0	1	2	3	4
Relay K_1	ON				
Relay K_2		ON			
Relay K_3			ON		
Relay K_4				ON	
Relay K_5					ON
A group	RESET	HOLD	HOLD	HOLD	HOLD
B group	H	R	H	H	H
C group	H	H	R	H	H
D group	H	H	H	R	H
E group	H	H	H	H	R

Fig. 3.24 Logic Mode Controls